Interleaving is Good for Boost Converters, Too

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Long used to improve efficiency, reduce ripple, and shrink capacitor and inductor size in buck converters, the multiphase approach can provide the same benefits for boost converters.

There have been many articles describing the use of multiphase buck converters, especially for high-performance point-of-load applications. However, all the advantages of interleaving, such as higher efficiency and reduced input and output ripple, are also realized in the boost topology. Most of the controllers used in buck applications apply equally well when configured for use in an interleaved boost application.

As power densities continue to rise, interleaved boost designs become a powerful tool to keep input currents manageable and increase efficiency, while still maintaining good power density. With mandates on energy savings more common, interleaved construction may be the only way to achieve design objectives. The benefits of this approach are demonstrated by a two-phase boost converter design built around the LM5032 pulse-width modulation (PWM) controller.

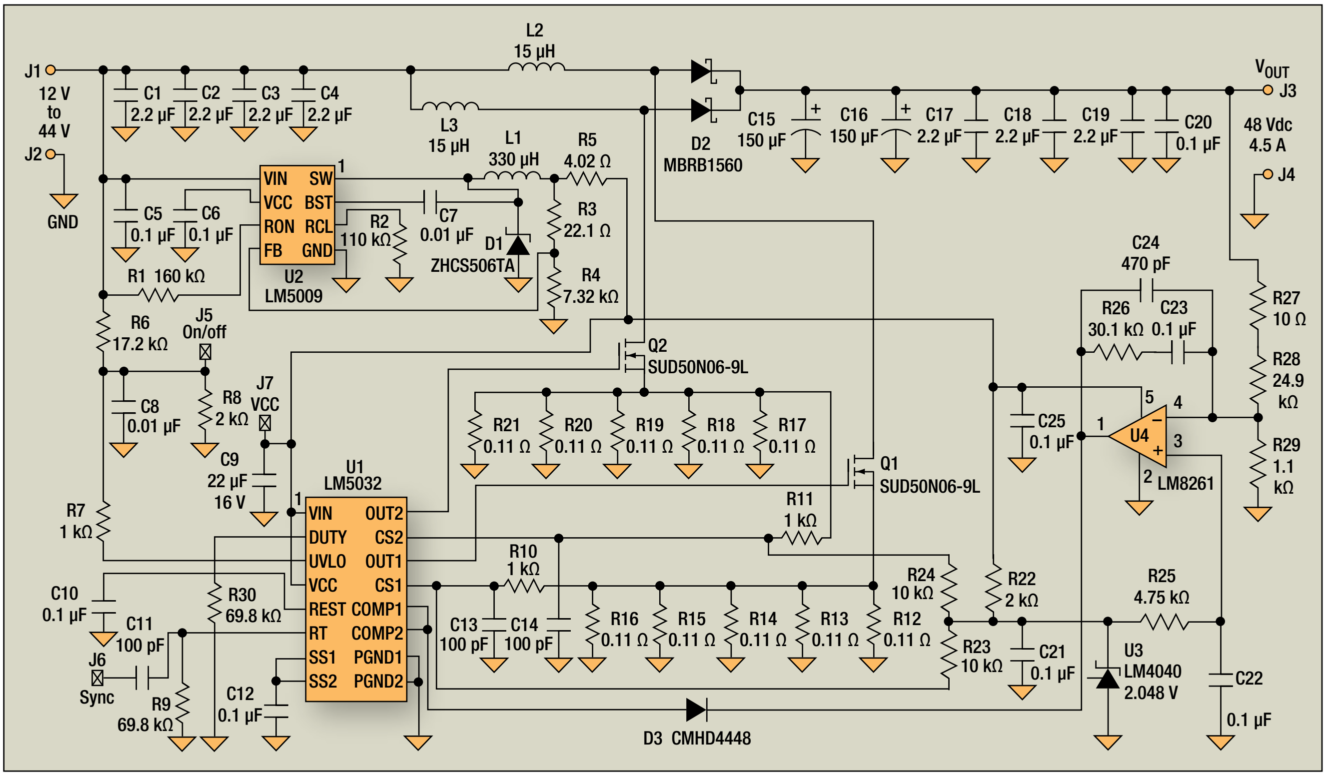

Fig. 1. *A two-phase boost converter built around a current-mode PWM controller (U1) generates 48 V at up to 4 A, while operating from an input of 12 V to 42 V.*

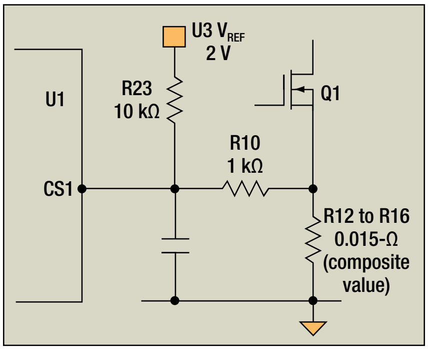

Fig. 2. *Adding this current-sense offset circuit, which produces 185 mV, to the circuit in Fig. 1 permits the use of lower-value sense resistors and lowers losses in each phase.*

Two-Phase Operation

In a two-phase converter, there are two output stages that are driven 180 degrees out of phase. By splitting the current into two power paths, conduction (I^2R) losses can be reduced, increasing overall efficiency compared to a singe-phase converter. Because the two phases are combined at the output capacitor, effective ripple frequency is doubled, making ripple voltage reduction much easier. Likewise, power pulses drawn from the input capacitor are staggered, reducing ripple current requirements.

As in the buck counterpart, the designer has the choice of achieving higher efficiency by using the same rated components as in an equivalent single-phase converter, by reducing component sizes to lower costs or by using some combination of these two approaches.

In the example described here, a boost converter is needed to generate a 48-V supply with high efficiency for a telecom application. The converter must be able to operate over a wide input-voltage range to accommodate a variety of input sources including batteries. Because of the wide input range, the converter also must be able to operate with a wide input-voltage to output-voltage ratio.

Here, the boost MOSFETs and inductors are sized for 12 A of input current. The output capacitors are chosen to limit output-voltage ripple to 500 mV (1%) or less. Overall, the goal is to push the efficiency to a high-enough level to allow operation at room temperature with no airflow, while still meeting all the other requirements. Specifically, the design goals are: V_{IN} = 12 V to 44 V, V_{OUT} = 48 V, I_{LOAD} = 4 A, $V_{RIPPLEOUT}$ < 500 mV, P_{OUT} = 192 W and efficiency > 95%.

Fig. 1 shows the schematic of the boost converter. The circuit is built around a two-phase current-mode PWM controller (U1) with separate inputs for current limit and compensation for each channel. Using current-mode control ensures the two channels share current closely.

Both channels are fabricated within the same IC, so even the lot-to-lot variations are minimized. The separate inputs for the PWM comparator are combined in this design, because we are implementing a two-phase single-output converter, not two independent converters.

The two current-sense inputs are used to keep the current balanced in each phase. Each output phase drives its own

power channel consisting of switching MOSFETs Q1 and Q2 and inductors L2 and L3. Output diode D2 is a dual common-anode device that feeds the common bank of output capacitors C15 to C19. The IC is internally configured to drive its two outputs 180 degrees out of phase.

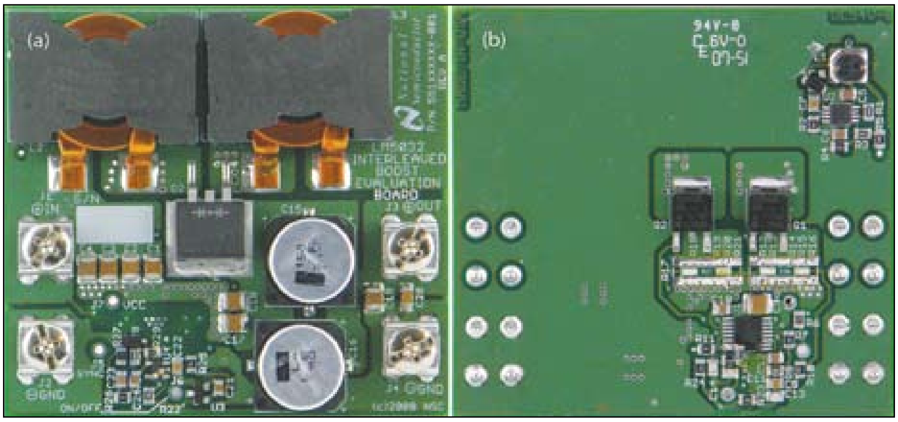

Fig. 3. *In this boost converter prototype, the PWM controller, power inductors and Schottky rectifier are placed on top of the board (a), while the bias supply and the switching MOSFETs are located on the bottom of the board (b) to complete a compact design.*

A single feedback network consisting of error amplifier U4 and associated passive-loop compensation components drive both comparator (COMP) inputs on U1, which are tied together at the IC.

To reduce the sense-resistor losses, a dc offset circuit (Fig. 2) was introduced to offset the current-sense inputs by 185 mV. This allowed the use of lower-value sense resistors in each phase, reducing I^2R losses.

Reference U3 is already in use as the error amplifier reference. Resistors R23, R18 and the current-sense resistors form a voltage divider from the 2-V reference. With the values from Fig. 1, the dc offset is 0.185 V, effectively reducing the current-limit threshold of 0.5 V by that amount. As long as R23 is much larger than R18, and with R18 much larger than the sense resistors, the dc offset will not adversely interact with the actual sensed current waveform. More offset could be used; however, compressing the actual current signal could introduce noise issues if taken too far.

To further reduce losses, a switching bias supply was constructed with adjustable controller U2. As can be seen from the photograph of the actual prototype in Fig. 3, this circuit is very small and offers a good solution for a bias supply. The prototype board measures 2.6 in. × 2.4 in.

If a linear regulator or zener diode were used, it would

be necessary to drop about 31 V from the input supply at $V_{IN_{MAX}}$. By supplying the necessary bias with an overhead current of 500 mA, a loss of about 16 W was avoided.

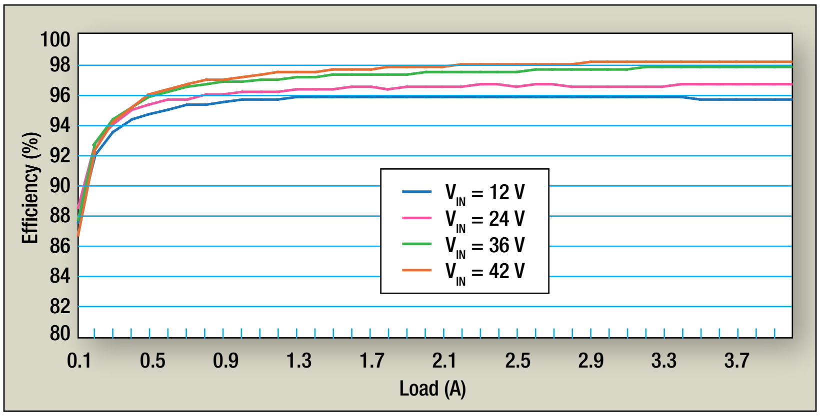

Fig. 4. *Measurements taken on the boost converter prototype attest to the fact that a compact boost design can also achieve high efficiency.*

Diode D3 prevents the error amplifier from holding the comp pin of U1 high during startup, effectively configuring the error amplifier as sink only. The PWM controller contains a 5-kΩ pull-up resistor.

A prototype of the circuit in Fig. 1 is pictured in Fig. 3. Here, the two power inductors occupy the top part of the left photograph, with rectification accomplished with the common-cathode Schottky diode located just below the inductors. The LM5032 PWM controller is located in the lower left portion of the board.

On the bottom side of the board in Fig. 3, the bias supply is located near the upper right, with the two switching FETs at center right. The error amplifier is located near the top left of the board. No heatsinking other than the copper in the pc board is used. A four-layer board was used for compactness of design and heat-dissipation properties.

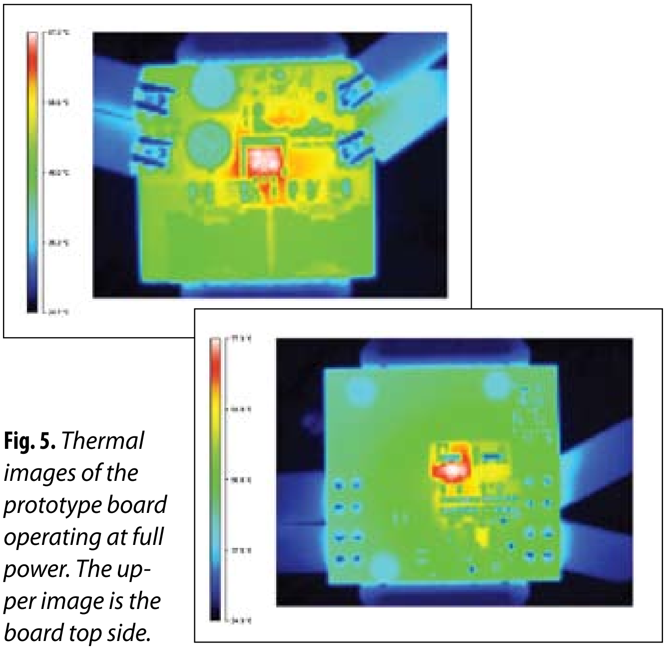

Fig. 5. *Thermal images of the prototype board operating at full power. The upper image is the board top side.*

Operational Results

Referring to the plots in Fig. 4, using data from the actual prototype, efficiencies range from 95% to 98% up to the full load current of 4 A, and over a 3.5:1 input-voltage range. In the very low current region (less than 200 mA) where overhead-bias currents dominate, the converter does have less efficiency, but this is true for all regulators. These plots illustrate the possibility of building a compact, high-power boost converter without sacrificing excellent efficiency.

Referring to the thermal images in Fig. 5, the component with the maximum temperature is Q2, which is operating at a case temperature of 77°C. Q2 is hotter than Q1 since it is directly opposite D2, which also dissipates considerable heat. Since the junction-to-case thermal resistance of Q2 is 1°C/W, and since Q2 dissipates about 4 W maximum, its junction temperature is about 81°C. The ambient temperature is 25°C. Q2 is the hottest component on the board, and is well within its thermal rating. Refer to the board photos in Fig. 3 for location of components.

Input and output ripple reduction are some of the benefits of an interleaved converter. Since the output ripple is double the frequency of the individual phases and at a lower root-mean-square (rms) current value, the designer has the choice of using smaller output capacitors with the same ripple as a single-phase converter or using larger capacitors to achieve even lower output ripple.

Effective ripple is a function of duty cycle. Using data from the actual prototype, Figs. 6 and 7 illustrate the input and output ripple currents versus duty-cycle relationships. Ripple reduction is a function of duty cycle, as the degree of ripple overlap is a function of duty cycle. There is near-perfect cancellation of ripple at 50% duty cycle. This opens the intriguing possibility of building a converter with little

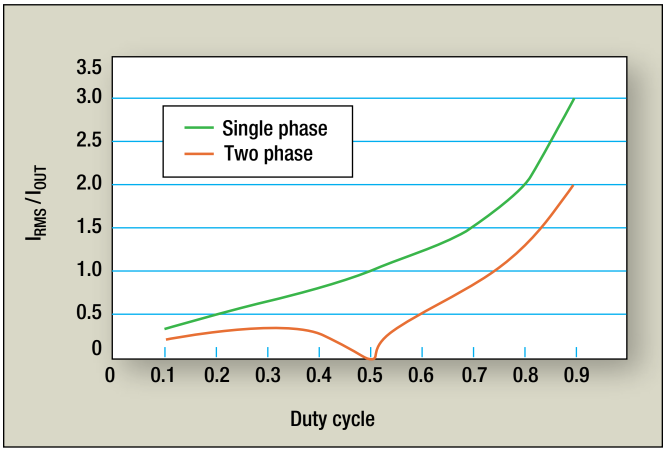

Fig. 6. *Normalized input-capacitor rms ripple current is measured as a function of duty cycle. Although the output capacitor must be chosen to withstand high ripple current inherent in any boost design, the capacitor can be significantly smaller in a two-phase design than in a single-phase implementation.*

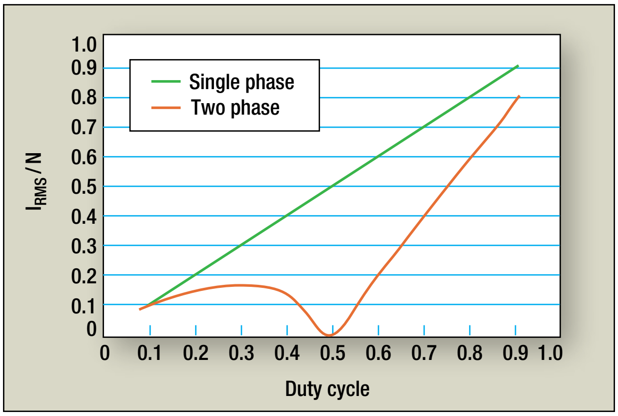

Fig. 7. *The normalized input-capacitor rms ripple current is measured as a function of duty cycle. Normalization factor N is given by* $N = V_{IN}/(L \times f_S)$.

to no output ripple if the designer can limit V_{IN} to the proper value for 50% duty cycle.

In the more general case, ripple is reduced by as much as 50% compared to an equivalent-power single-phase converter. Likewise, inductor selection is flexible with the two-phase design. One-half the single-phase inductor value can be chosen, which will make each inductor smaller, but which results in the same ripple currents as the single-phase design. Or the inductors can remain the same value as in the single-phase design, reducing the ripple by one-half.

The proper tradeoffs will depend on the overall design goal. Attention to ESR requirements will keep capacitors within temperature ratings and the output voltage ripple within specifications.

Fig. 6 plots normalized output capacitor ripple current versus duty cycle. This graph shows the ripple cancellation at 50% duty cycle and the general ripple reduction across all duty cycles with the two-phase topology. The output capacitor must be chosen to withstand the high ripple current inherent in a boost design. However, as can be seen in Fig. 6, it can be significantly smaller than in a single-phase implementation.

Fig. 7 plots normalized input-capacitor ripple current versus duty cycle. In this case, the normalization is chosen to simplify the graph scale.

This prototype illustrates that the many benefits of interleaving, which are routinely used in buck regulators, apply equally well to an interleaved boost design. In the design presented here, the impressive power-conversion efficiency results in a 192-W, all-surface-mount design that will operate without airflow at room ambient.

This design could easily be upgraded to higher power by the proper selection of power components. Also, since the selection of output voltage and input voltage are at the designer's discretion, the basic design could be adapted to many battery-powered applications. By overdesigning the power components and/or reducing the switching frequency, efficiency could be improved if that were the primary design goal. **PETech**