FEATURE ARTICLE

Valley Design Techniques Outperform Peak Current-Mode Approach for CPU

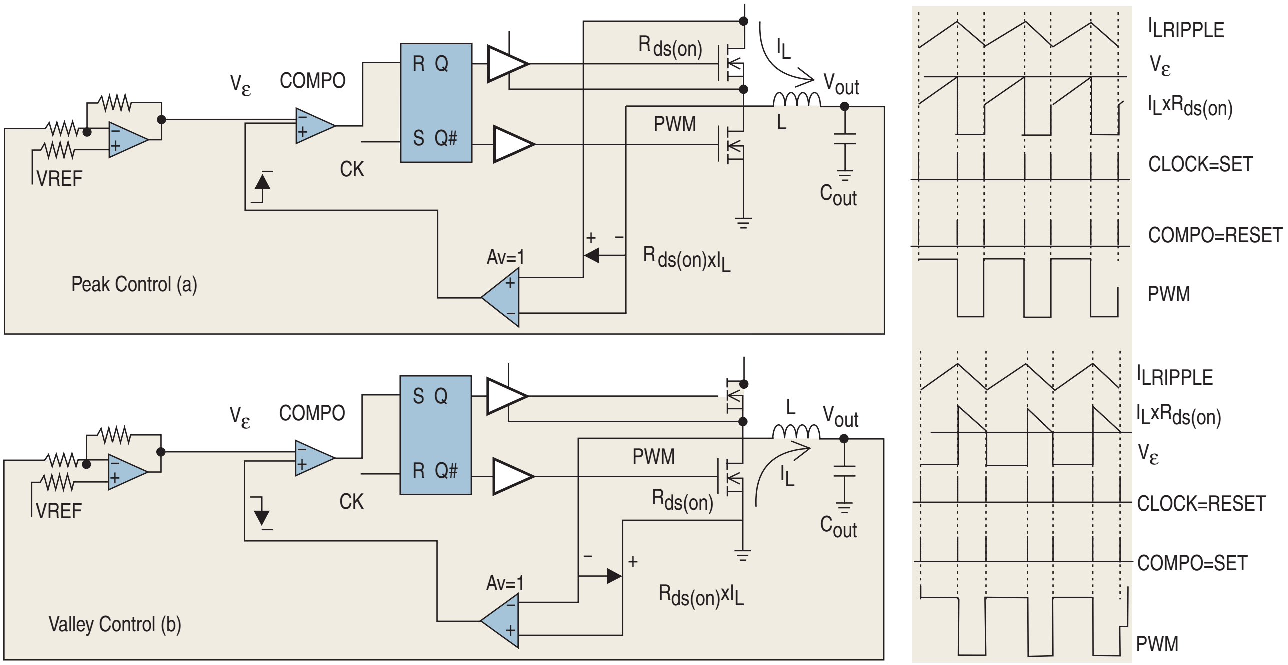
Valley current-mode control has superior regulation and transient response compared with traditional peak current-mode control.

By Nazzareno Rossetti, Fairchild Semiconductor, San Jose, Calif.

Modern CPUs require supply voltages of 1.5V and below and currents of up to 100A. This power frequently originates from the 12V output of a "silver box" power supply. Developing the lower voltage requires a buck converter operating at duty cycles of about 10%, stretching the performance limits of conventional current-mode control architectures. Valley current-mode allows the buck converter to meet and exceed those specifications.

To understand the valley current-mode control, we first have to look at traditional peak current-mode control in **Fig. 1(a),** which is based on trailing-edge modulation. In closed-loop operation, the error amplifier forces V_{OUT} to equal V_{REF}. At the error amplifier's output, its output voltage V_ε is compared with the product of the high-side MOSFET's current (I_L) times $R_{DS(on)}$. When $I_L \times R_{DS(on)}$ exceeds the error voltage, the PWM comparator goes high. This resets the flip-flop, terminating the charge phase by turning off the high-side driver and initiating the discharge phase by turning on the low-side driver. The discharge phase continues until the next clock pulse that sets the flip-flop and initiates a new charging phase.

Fig. 1(b) illustrates valley current-mode control based on leading-edge modulation. The error amplifier again forces



Figs. 1(a) and (b). *Peak vs. valley current-mode control.*

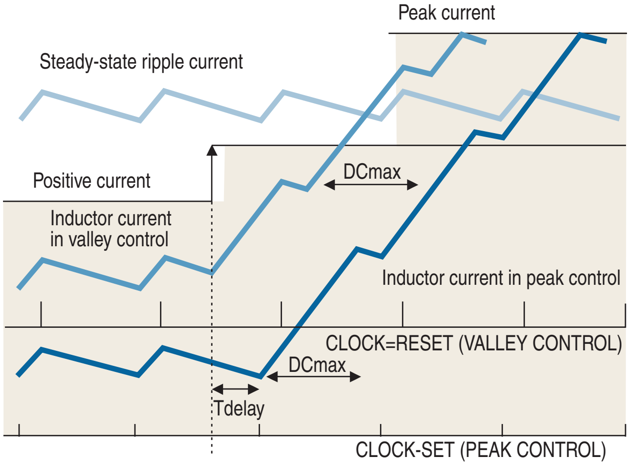


Fig. 2. *Comparison of response to a positive current step.*

V_{OUT} to equal V_{REF} at its input. But now its output voltage, V_{ε}, is compared with the low-side MOSFET's current (I_L) times $R_{DS(on)}$. When $I_L \times R_{DS(on)}$ falls below the error voltage the PWM comparator goes high. This sets the flip-flop, initiating the charge phase by turning on the high-side driver and terminating the discharge phase by turning off the low-side driver. The charge phase continues until the next clock pulse resets the flip-flop, initiating a new discharge phase.

Current Sensing

"Lossless" current sensing employs no discrete sense resistor, sensing instead the voltage across the low-side MOSFET—which is ON normally for 90% of the time. Because the ON time of the low-side MOSFET is almost 10 times longer than that of the high-side MOSFET, sampling and processing of the low-side device's current is much easier.

Sensing of the high-side current at low duty cycles is so difficult that some designs have been based on sensing low-side current and trailing-edge current control. However, the current information obtained this way comes after the current has peaked and has started the decaying phase—allowing only cycle-by-cycle peak-current control during the next cycle. This means you hold the sampled information until the next cycle. A sample-and-hold mechanism adds

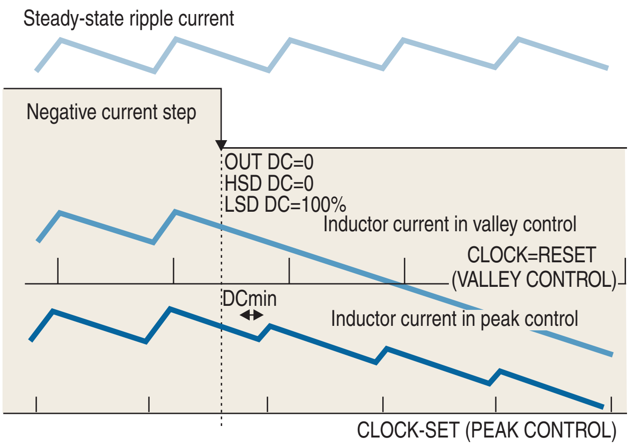


Fig. 3. *Comparison of response to a negative current step.*

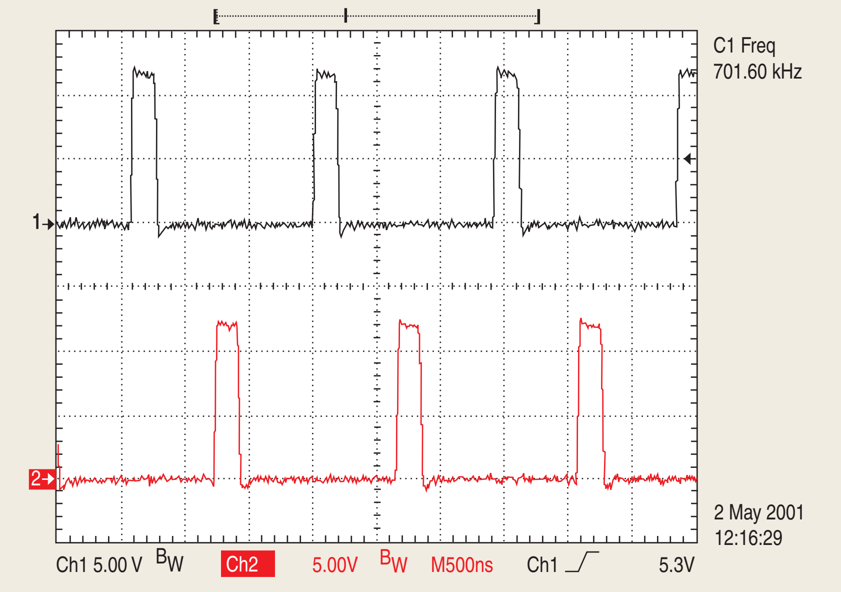


Fig. 4. *Interleaved buck converter:* $V_{IN} = 12V$; $V_{OUT} = 1.5V$; $f_{CK} = 700$ *kHz per phase.*

complexity and a delay or phase shift, which can compromise the control loop's stability.

For valley or peak current-mode control, in the case of very low duty cycle operation, the minimum possible ON time of the high-side driver limits the maximum frequency of operation. In both cases you determine the high-side driver's minimum pulse width by the same set of initial physical limitations, and the peak current-mode control's maximum frequency is limited by a settling-time requirement. The pulse must be wide enough to allow you to measure the current. This limitation applies to both lossless high-side sensing and to sensing with a discrete high-side sense resistor.

[redacted]

Peak Currnt-Mode Control

For peak current-mode control:

$T_{MINP}=T_{ONP\text{-}MIN}/DC$ (1)

Where:

T_{MINP}=Minimum period of operation in peak current-mode control

$T_{ONP\text{-}MIN}$=Settling time for sensing the high-side current

DC=Duty Cycle

If $T_{ONP\text{-}MIN}$=100 ns and DC=0.1:

T_{MINP}=100 ns/0.1=1 µs

And:

$f_{MAXP}=1/T_{MINP}$ (2)

Where:

f_{MAXP}=Maximum operating frequency in peak current-mode control

f_{MAXP}=1 MHz

Valley Current-Mode Control

In valley current-mode control where the low-side current is sampled, the limitation discussed above is far less strict. $T_{MINV}=T_{ONV\text{-}MIN}/(1\text{-}DC)$ (3)

Where:

T_{MINV}=Minimum operating period in valley current-mode control based on low-side minimum pulse width.

$T_{ONV\text{-}MIN}$=Settling time for sensing the low-side current

If $T_{ONV\text{-}MIN}$=100 ns and DC=0.1:

T_{MINV}=100 ns/(1-0.1)=110 ns

And: $f_{MAXV} = 1/T_{MINV}$ (4)

Where:

f_{MAXV}=Maximum operating frequency

f_{MAXV}=1/110 ns=9 MHz

The converter still has to meet the constraint of minimum ON time of the high-side driver. Transition times of 10 ns and below are obtainable today. Therefore:

$T_{ONHV\text{-}MIN}=T_R+T_F$ (5)

Where:

$T_{ONHV\text{-}MIN}$=Minimum ON time of the

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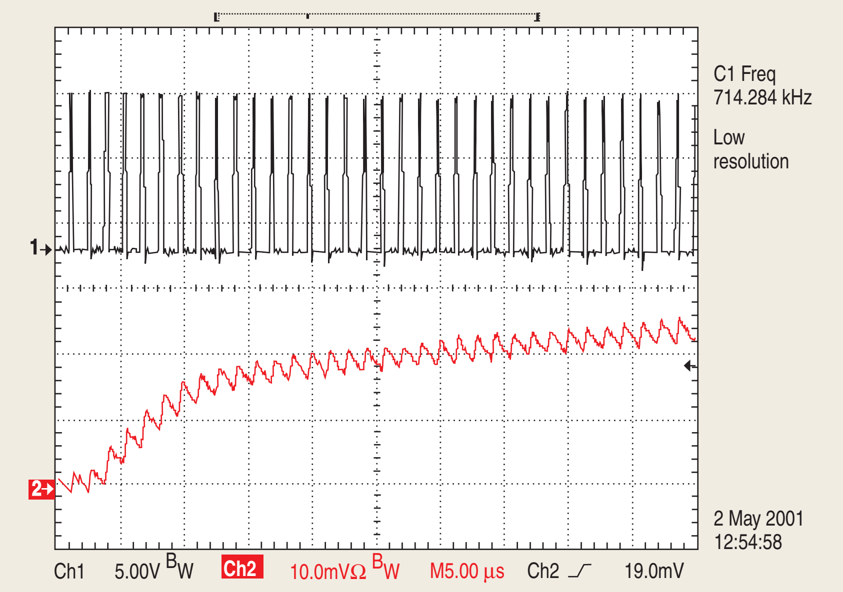

Fig. 5. *Regulator response to a positive current step: a) Top waveform: switching node of Phase 1; b) Bottom waveform: Phase 1 current.*

high side device

T_R=Rise time in nanoseconds

T_F=Fall time in nanoseconds

$T_{ONHV\text{-}MIN}=10+10=20$ ns

Also:

$$T_{MINHV}=T_{ONHV\text{-}MIN}/DC \qquad (6)$$

Where:

T_{MINHV}=Minimum operating period in valley current-mode control based on high side minimum pulse width.

$T_{MINHV}=20 \text{ ns}/0.1=200$ ns

And:

$$f_{MAXHV}=1/T_{MINHV} \qquad (7)$$

f_{MAXHV}=Maximum operating frequency in valley current-mode control based on high side minimum pulse width.

$f_{MAXHV}=1/T_{MINHV}=5$ MHz

The most severe constraint is the high side minimum pulse width, which for valley current-mode control still translates into a high maximum clock frequency (f_{MAXHV}) of operation.

Conventional monolithic and discrete technologies don't permit practical operation at such a high clock rate. As these technologies improve, only valley current mode control will operate at such high frequencies.

Transient Response

The advantage of valley control is obvious in **Fig. 2,** on page 51. It can turn on immediately in response to a step current as opposed to peak control where a delay (T_{DELAY}) as high as a full clock period is to be expected.

Both cases show the inductor current ramps up with a slope determined by the inductance and saturated voltage appearing across the inductor, limited by the maximum duty cycle DC_{MAX}.

If the clock is 700 kHz per phase, a full period delay corresponds to 1.5 ms. A traditional peak current-mode control architecture needs enough output capacitance to hold up for an extra 1.5 ms compared with valley current-mode control. Consider that a 1 µF output capacitor will discharge an extra 100mV with a 65A load in 1.5 µs.

Fig. 3, on page 51, illustrates the comparative responses to a negative load current step. During a negative load-current step, the valley control scheme responds with zero delay. With peak current-mode control, after each clock pulse, the controller forces a minimal width high-side ON time. The speed of the current control loop determines minimal ON time. The valley control scheme offers superior transient response with a negative load step.

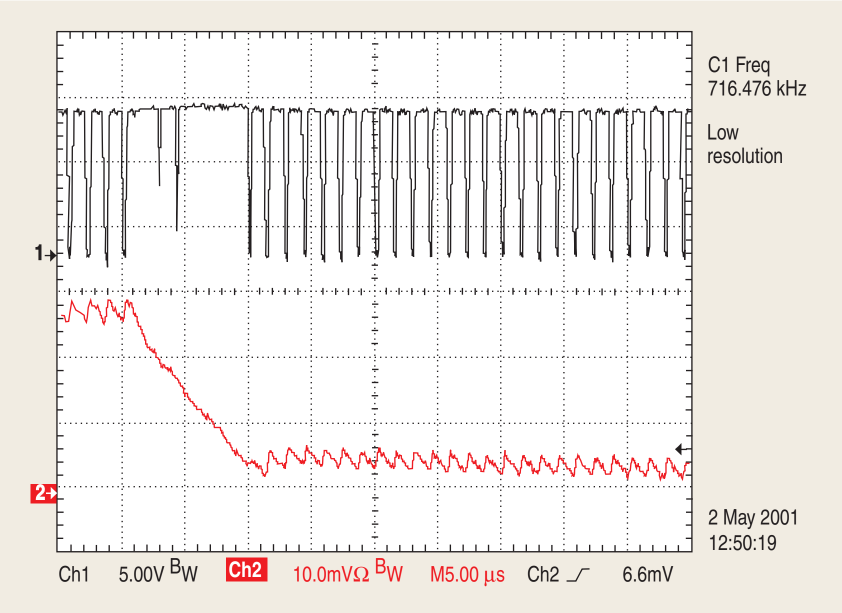

Fig. 6. *Regulator response to a negative current step: a) Top waveform: switching node of Phase 1; b) Bottom waveform: Phase 1 current.*

Valley Control IC

The FAN5093 is a 2-phase interleaved buck controller IC implementing valley control architecture based on leading-edge modulation. The current is normally sensed across the low-side MOSFET's $R_{DS(on)}$ (for lossless current sensing). For precision applications, you can place a physical sense resistor in series with the source of the low-side MOSFET.

Looking at **Fig. 4**, on page 52, you can see the response of the two PWM switching nodes of the 2-phase interleaved buck converter, with the FAN5093 clocking each phase at a frequency of 700 kHz.

Fig. 5, on page 55, is the response of the voltage regulator to a 25A per phase positive current step. You can see the response of the voltage regulator to a 25A per phase negative current step in **Fig. 6**. **PCIM**

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