

Power Converter Synthesis— Part 3: Near Zero Emissions

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Parts 1 and 2 of this series describe synthesis methods that achieve improved EMC properties for nonisolated converters. In this part, let's apply similar synthesis methods to isolated full- and half-bridge circuits.

While a conventional full-bridge forward converter circuit has pulsating input current that generates conducted differential mode noise at the line terminals, it also offers a high degree of balance that accomplishes first order cancellation of displacement currents (Fig. 1). Recall that the displacement current is given by $I_D = C_{PARA} \times dV/dt$, where I_D is the displacement current, C_{PARA} is the parasitic capacitance at the node that generates the displacement current, and dV/dt is the voltage rate of change of the node that generates the displacement current.

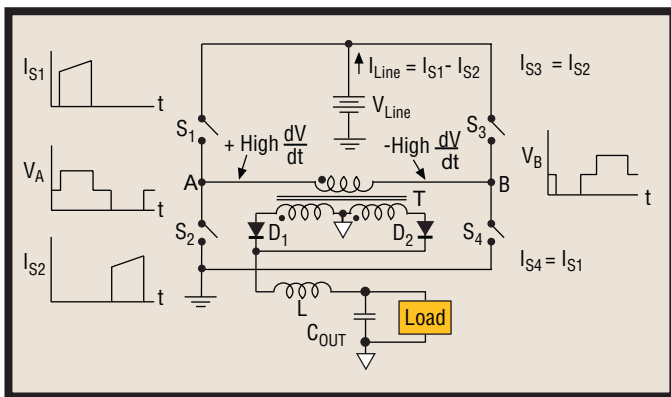


Fig. 1. A PWM full bridge forward converter.

The voltage waveforms at nodes A and B are equal in magnitude but 180° out-of-phase so that the nodes A and B form a dipole for radiation of electric fields. Dipole radiators are superior to monopole radiators because they provide an effective first order electric field cancellation in the far field. This inherent balance gives the full bridge circuit a common mode noise performance advantage compared to some other converter types. There's also a high order of balance in the secondary circuit.

Synthesis of Bridge Converters

Fig. 2(a), on page 36, illustrates the full-bridge forward converter of Fig. 1. The Fig. 2(b) circuit splits the primary winding of the transformer into two equal series connected windings, each with half the number of turns of the original primary winding. The Fig. 2(c) circuit splits each of the primary windings into two equal parallel connected windings, each with same number of turns as the original windings, but with half the number of strands as the original windings. The transformations to Figs. 2(b) and 2(c) are possible based on the reasoning asserted in key point No. 2 of Part 1 of this article series. The Fig. 2(d) circuit disconnects the switch end terminals of the parallel connected windings. The winding voltages, the average winding currents, and the total net primary winding current in the Fig. 2(d) circuit are the same as the winding voltages, the average winding currents, and the total net primary winding current in the Fig. 2(c) circuit. However, the instantaneous winding currents in the Fig. 2(d) circuit are different from the instantaneous winding currents in the Fig. 2(c) circuit.

In Fig. 2(d) the current in each winding is equal to the current in the switch that's connected in series with the winding. The Fig. 2(e) circuit is the same as the Fig. 2(d) circuit, but the positions of switches and windings are reversed in their series connections. The transformation to Fig. 2(e) is possible based on the reasoning asserted in key point No. 4 of Part 1 of this article series. Fig. 2(f) adds two capacitors to the Fig. 2(e) circuit. Key point No. 6 of Part 1 of this article series suggests that we can add capacitors C_1 and C_2 and that the applied voltage to each capacitor will be equal to the line voltage. The capacitors provide a preferred path for ac switch currents and a path for dc winding currents when the switch associated with that winding is off. The windings provide a preferred path for dc currents, although each winding has both a dc and an ac component.

The waveforms for the switch currents, illustrated in

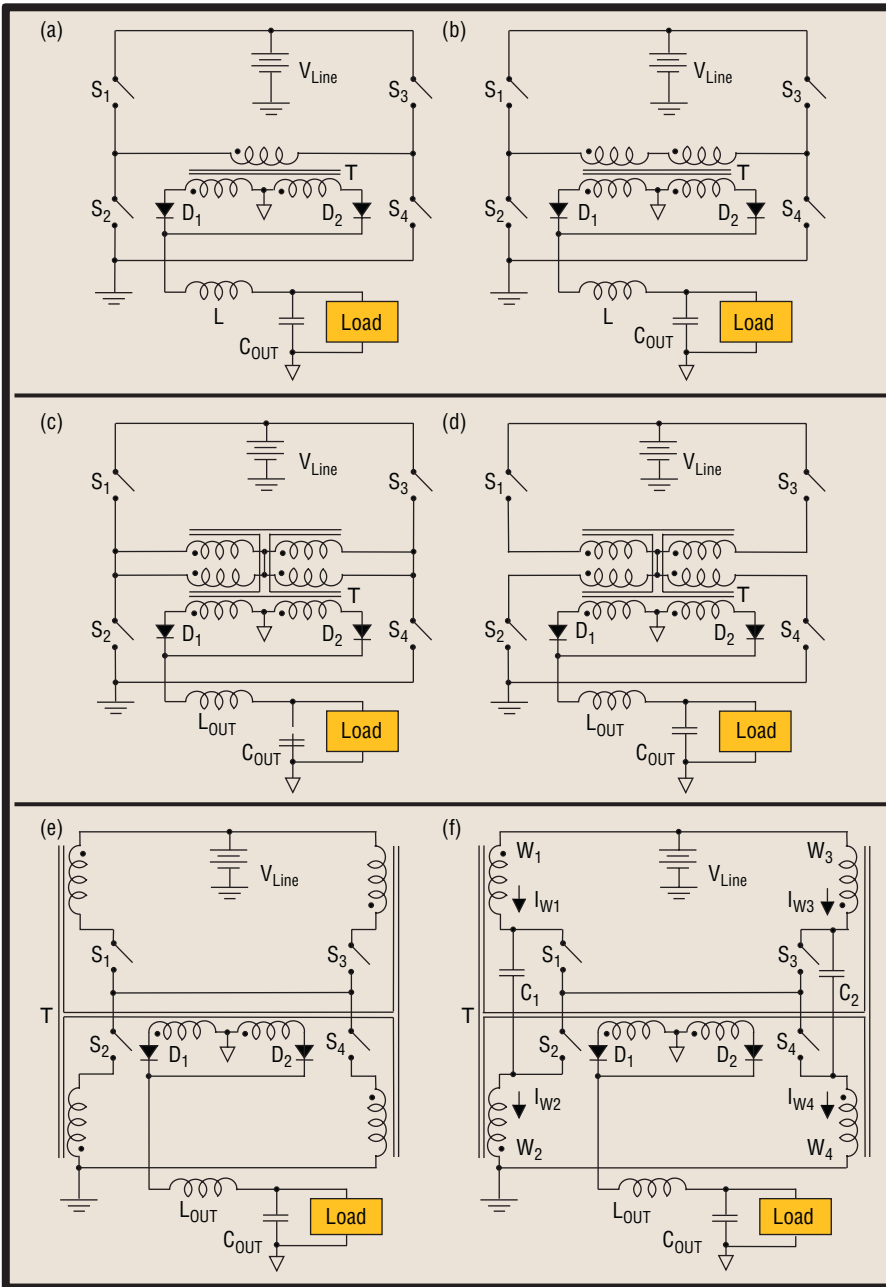


Fig. 2(a). A PWM full-bridge forward converter, **(b)** the same converter with its transformer primary winding split into two series windings, **(c)** the same converter with the two primary windings split into two parallel windings, **(d)** the same converter with the switch terminal ends of the windings disconnected from each other, **(e)** the same converter with the switch and winding positions reversed in their series connections, **(f)** the same converter with two capacitors added to achieve terminal ripple current cancellation.

Figs. 3(a) and 3(b), on page 37, are unchanged from the original full-bridge circuit, but the winding structure and winding currents have changed considerably. Each winding in the Fig. 2(f) circuit has a dc component, but the total net dc primary current is the same as the original Fig. 2(a) circuit, and the average dc primary current is

zero. Figs. 3(d) and 3(e) illustrate the winding currents. The positive direction for each winding current is indicated in Fig. 2(f). At each line terminal, two windings are connected—one with its dotted terminal connected to the line terminal and one with its undotted terminal connected to the line terminal. The ac currents

in the two windings connected at each line terminal are equal in magnitude but opposite in direction, so that the net ac current at each line terminal is zero (i.e., the line terminal ripple currents for the two windings cancel). This result is suggested by key point No. 1 of Part 2 of this article series. Fig. 3(f) illustrates this result for the line terminal current. Consider the case for which switches S_1 and S_4 are on and switches S_2 and S_3 are off. The dotted terminal of each winding is forced positive with respect to the undotted terminal of each winding and the current ramps up in each winding from the dotted terminal to the undotted terminal, assuming that the capacitors are large and the capacitor voltages are equal to the line voltage and invariant. If we consider the positive line terminal, then the line current is ramping up due to the current ramping up in winding W_1 and the line current is ramping down due to the current ramping down in winding W_3 . During the time that one pair of switches is on, capacitors C_1 and C_2 are discharging into the switches. During the time that all switches are off, capacitors C_1 and C_2 are charging, thereby maintaining the dc winding currents and providing a path for dc line current while the switches are off. The result of this synthesis process is a full-bridge forward converter equivalent in every way to the original conventional full-bridge forward converter, but with reduced conducted differential mode emissions.

The synthesis process added two capacitors and changed the winding structure of the isolation transformer. The new isolation transformer requires six primary terminals rather than two terminals in the original transformer, but no increase in window area or core cross section is required. The original circuit has an inherent balance so that displacement currents due to the high dV/dt nodes are self canceling to a first order approximation. The new circuit created by the synthesis process preserves this property and improves on it since the ac voltage magnitudes are half that of

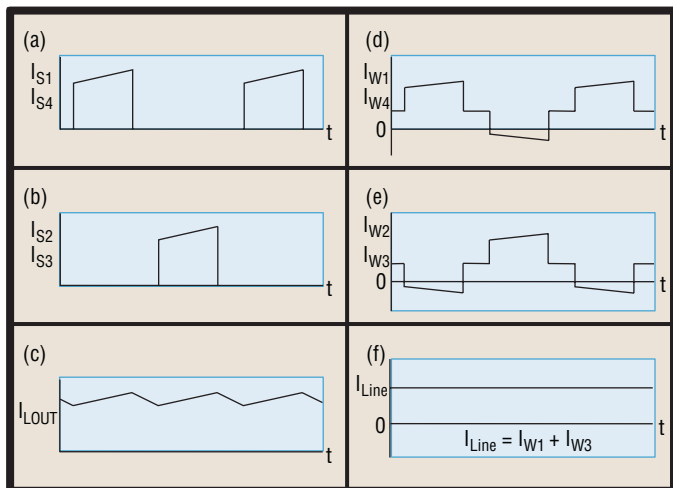


Fig. 3(a). Switch S_1 and S_4 current, **(b)** switch S_2 and S_3 current, **(c)** output choke current, **(d)** winding W_1 and W_4 current, **(e)** winding W_2 and W_3 current, **(f)** line current.

the original circuit and there are now four ac voltage nodes rather than two.

Fig. 4(a), on page 40, illustrates a half-bridge forward converter similar in structure to the full bridge forward converter, except that the half-bridge circuit has two ca-

pacitors in the right leg of the bridge that replace the right leg switches of the full bridge. One significant performance difference between the half-bridge circuit and the full-bridge circuit is that the half bridge has only one high dV/dt node so that the inherent balance in the full bridge circuit is absent in the half bridge. The single high dV/dt node in the Fig. 4(a) circuit is the node that connects the two switches and the primary winding of the transformer. The synthesis process described above for the full bridge can be applied to the half-bridge circuit. The result of the synthesis is the Fig. 4(b) circuit.

Figs. 5(a) through 5(h), on page 40, illustrate waveforms for the Fig. 4(b) circuit. The waveforms for the left leg windings and switches are similar to the full-bridge circuit. However, the waveforms for the right leg windings are different because the right leg windings are ac coupled so there's no dc current component in the right leg windings, as illustrated in Fig. 5(f) and 5(g). The Fig. 4(b) circuit achieves the same terminal ripple current cancellation as was achieved by the Fig. 2(f) circuit for the same reason (i.e., the ac currents of the two windings connected at each line terminal are 180° out-of-phase). Another result achieved by the Fig. 4(b) circuit is that the Fig. 4(b) circuit contains multiple high dV/dt nodes, and the nodes to the left of the



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switches are out-of-phase from the nodes to the right of the switches. As a result, the displacement currents from the left side of the circuit cancel the displacement currents from the right side of the circuit. If the parasitic capacitances on the right side of the circuit are equal to those on the left side of the circuit, then the degree of cancellation will be more complete in the far field. The original circuit in Fig. 4(a) is a monopole radiator, and the Fig. 4(b) circuit is a dipole radiator. A quadrupole radiator can be created by

using a solid copper ground (image) plane. If the parasitic capacitances aren't well matched, then you can add small neutralizing capacitors to improve the balance and displacement current cancellation. Displacement currents can result in differential mode noise or common mode noise or both, depending on the receiving plates of the parasitic capacitances.

In general, common mode noise does more harm than differential mode noise and is more difficult and costly to eliminate. The largest para-

sitic capacitances are typically associated with semiconductor insulators on heatsinks, and winding-to-winding capacitances and winding-to-core capacitances in the isolation transformer. For low-voltage windings in an isolation transformer, the displacement current cancellation may be sufficient to obviate a faraday shield. However, in general, eliminating the faraday shield would be ill advised. Often, common mode noise is reduced on a heatsink or in a transformer by using a shield that effectively blocks the common mode displacement current path by creating a more direct differential mode displacement current path.

Reducing noise at its source is usually less costly than generating the noise at its source and then trying to eliminate it in other places and by other means. Typically, there's no limit to the amount of differential mode capacitance that can be added to eliminate differential mode noise, but common mode capacitance is often limited by restrictions on line frequency green wire currents imposed to prevent shock and personal injury. High-voltage isolation requirements are also often imposed by safety agencies, and common mode capacitors must be able to withstand the isolation voltage, thus increasing the size and cost of common mode capacitors. Common mode noise is also called antenna mode noise because over most of the noise frequency spectrum there's a high degree of correlation between common mode conducted emissions and radiated emissions.

In Fig. 2(f), switches S_1 and S_4 operate in synchronization and switches S_2 and S_3 operate in synchronization. These switch pairs are connected to each other and operate as though they are connected in series. When S_1 and S_4 are on, the undotted terminal of winding W_1 is connected to the dotted terminal of winding W_4 . When S_2 and S_3 are on, the dotted terminal of W_3 is connected to the undotted terminal of W_2 . When all the switches are off, none of the windings are connected to any of the other windings. This suggests that the switch pairs can

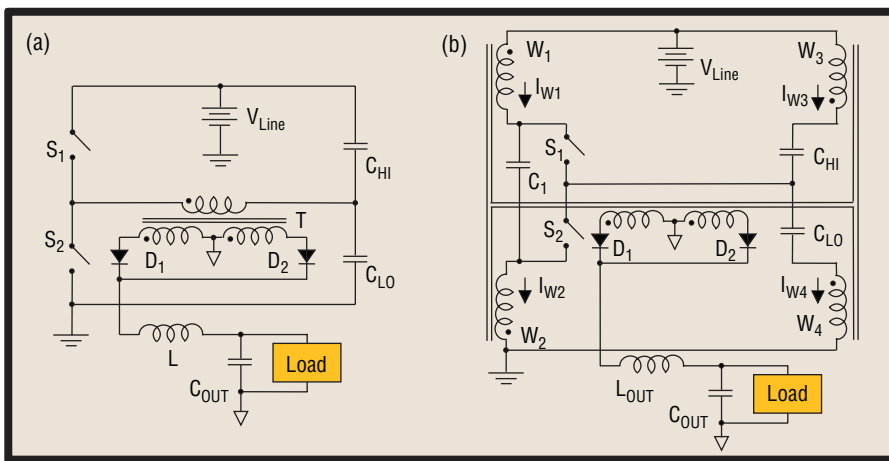


Fig. 4(a). A half-bridge forward converter, (b) the same half-bridge forward converter with the synthesis method applied to achieve terminal ripple current and common mode noise cancellation.

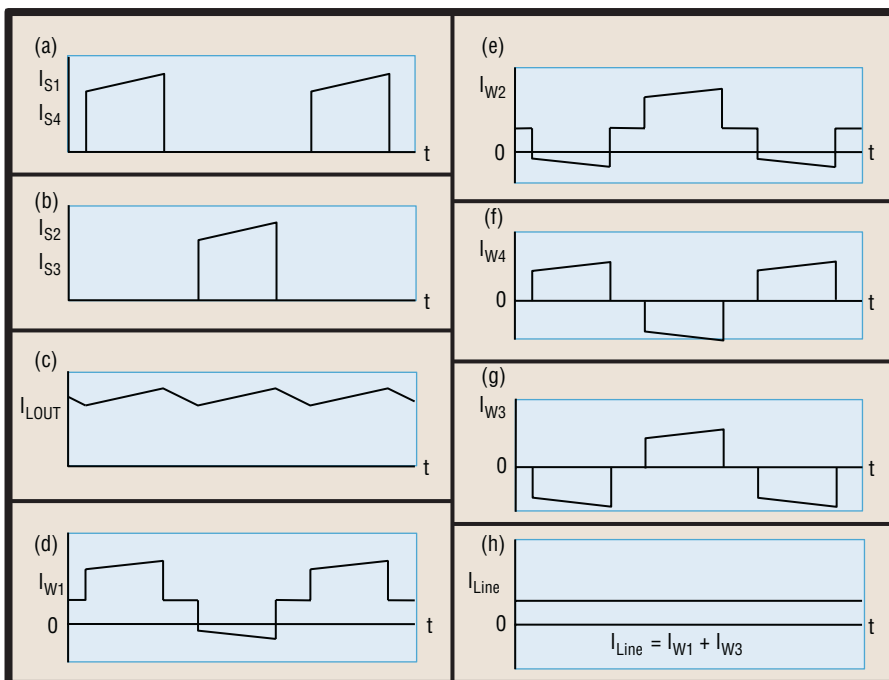


Fig. 5(a). Switch S_1 current, (b) switch S_2 current, (c) output choke current, (d) winding W_1 current, (e) winding W_2 current, (f) winding W_4 current, (g) winding W_3 current, (h) line current.

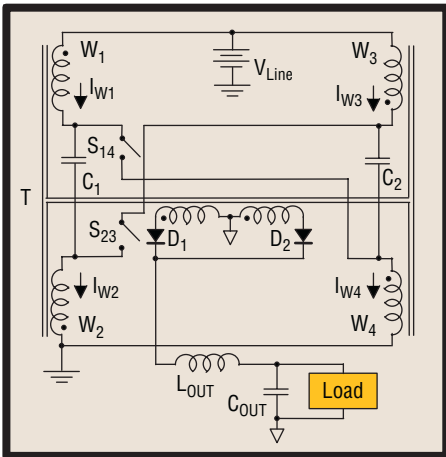


Fig. 6. A push-pull forward converter with terminal ripple current and common mode noise cancellation.

be combined to yield a circuit with only two switches (Fig. 6), with S_{14} connecting the undotted terminal of winding W_1 to the dotted terminal of W_4 , and with S_{23} connecting the dotted terminal of W_3 to the undotted terminal of W_2 . The new switches

must carry the same current but bear twice the applied voltage as one of the original switches in the Fig. 2(f) circuit, suggesting that the die for the new switches should be twice as large.

The circuit in Fig. 6 is actually a push-pull circuit, as will be shown in Part 4 of this article series. The Fig. 6 circuit maintains the terminal current and common mode noise properties of the Fig. 2(f) circuit, but reduces the switch count by half. The Fig. 6 circuit is actually well known and was first revealed in reference 4. References 1 and 2 provide more examples of EMC enhanced full- and half-bridge circuits. Reference 3 provides experimental data that shows the benefits of circuit balancing to common mode noise performance.

EMC Enhancing Synthesis Methods

In Part 4 of this series, we'll cover how you can apply EMC enhancing

synthesis methods to single-ended and push-pull isolated circuits. **PETech**

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