

Power Conversion Synthesis— Part 1: Buck Converter Design

By Ernest H. Wittenbreder, Jr., Technical Witts Inc.,
Flagstaff, Ariz.

A new buck converter design with improved terminal current and common mode noise results from the synthesis of power conversion circuits with nonpulsating input and output terminal currents.

Reducing emissions is a common goal when it comes to synthesis of power conversion circuits with nonpulsating input and output terminal currents. Emissions can result from pulsating currents due to magnetic coupling of the high dI/dt transmitting loop to nearby receiving loops. Noise mechanisms for a buck converter are shown in Fig. 1. The loop containing switch, Q, rectifier, D, and input capacitor, C_{XY} , experiences high dI/dt due to switch current pulses.

A receiving loop will have an induced EMF:

$$E_{DM} = M \times \frac{dI}{dt} \quad (1)$$

Where:

M = Mutual inductance between the transmitting loop and the receiving loop

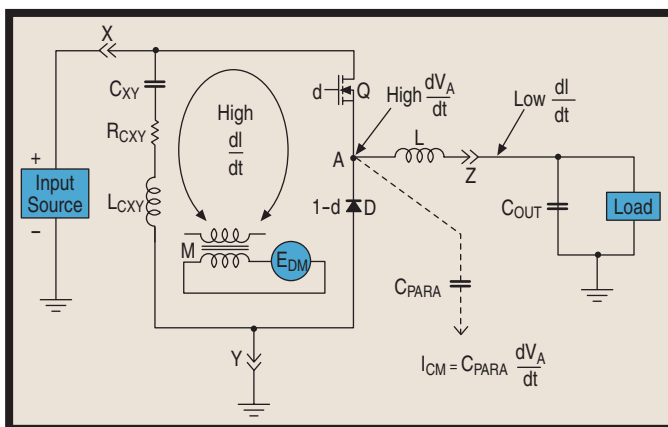


Fig. 1. Buck converter illustrating sources of electromagnetic emissions.

Noise induced in the receiving loop is typically differential mode noise. You can reduce the emissions by using a ground plane, and placing components and copper traces to minimize loop areas of both the transmitting and re-

ceiving loops.

Another source of differential mode emissions results from pulsating switch currents creating spikes across the equivalent series inductance (ESL), L_{CXY} , of the input capacitor. Voltage spikes occurring at the switching instants appear across the input capacitor, C_{XY} , due to high dI/dt and ESL:

$$V_{SPIKE} = L_{CXY} \times \frac{dI}{dt} \quad (2)$$

A lesser source of differential mode noise is the capacitor's equivalent series resistance (ESR). The effects of pulsating current, ESL, and ESR are illustrated in Fig. 2(a). At the output terminal of Fig. 1 emissions are low because current at the Z terminal is nearly dc, as illustrated in Fig. 2(b) and because the Z terminal current is nonpulsating due to the Z terminal inductor.

Key Point No. 1: Any current flowing through an inductor is nonpulsating, since a step current through an inductor implies an infinite voltage applied to the inductor.

Often, the most hideous source of noise emissions is common mode noise resulting from high transient voltages, i.e., high dV/dt . Circuit node A in Fig. 1 is a point of high dV/dt , as illustrated in Fig. 2(d). Parasitic capacitance at node A will transfer charge to other conducting surfaces. Common mode noise manifests itself as displacement currents in the parasitic capacitors formed by conducting surfaces with high dV/dt , so that:

$$I_{CM} = C_{PARA} \times \frac{dV_A}{dt} \quad (3)$$

Where:

I_{CM} = Displacement current

C_{PARA} = Total parasitic capacitance

dV_A/dt = Rate of voltage rise or fall at node A.

For Fig. 1:

$$\frac{dV_A}{dt} = \frac{V_I}{T_{TR}} \quad (4)$$

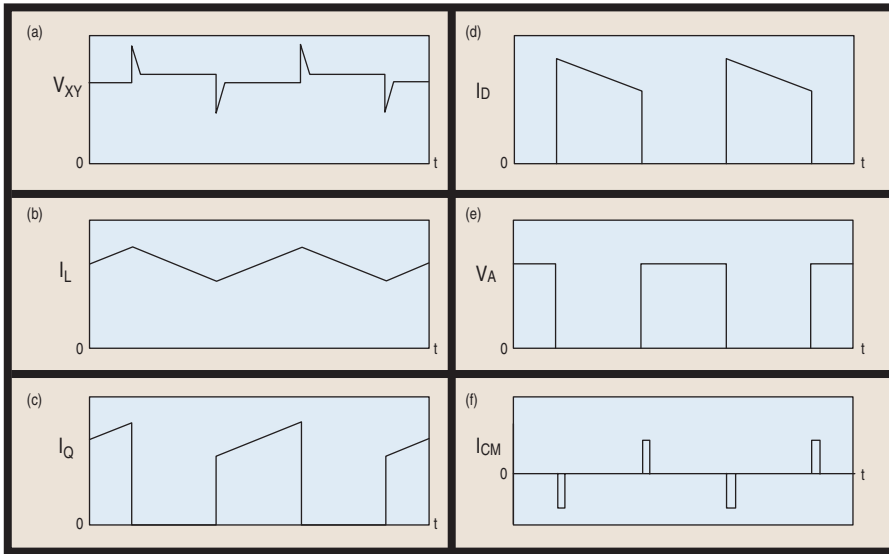


Fig. 2. Waveforms of the circuit in Fig. 1, (a) input capacitor C_{xy} voltage, (b) output choke current, (c) switch Q current, (d) diode D current, (e) node A voltage, (f) common mode current generated at node A.

Where:

V_i = Input source voltage

T_{TR} = Transition time

The waveform for node A is illus-

trated in Fig. 2(e). Common mode noise is minimized by reducing surface areas of unshielded conductors connected to the node A. Common mode currents resulting from parasitic capacitance at node A are illustrated in Fig. 2(f).

Converter Synthesis

Fig. 3(a) illustrates a buck converter. In Fig. 3(b), we split the inductor winding into two series connected windings.

Key Point No. 2: A series or parallel combination of circuit elements of the same type can be replaced by an equivalent single circuit element of the same type and a single circuit element can be replaced by a series or parallel combination of circuit elements of the same type in the reverse process.

In Fig. 3(c), we split one of the two series windings into two parallel windings with equal turns.

Key Point No. 3: If there are two inductors in the same circuit and the ac winding voltages of the two inductors are proportional to their turns ratio at all times, then the two inductors can be wound on a single common magnetic core.

The two parallel windings must have the same number of turns for the connection illustrated in Fig. 3(c).

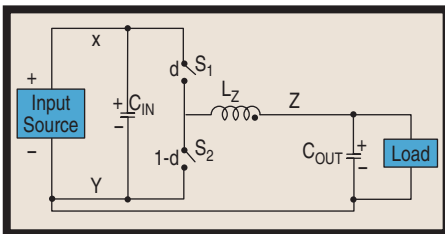


Fig. 3a. Synthesis process: original buck converter.

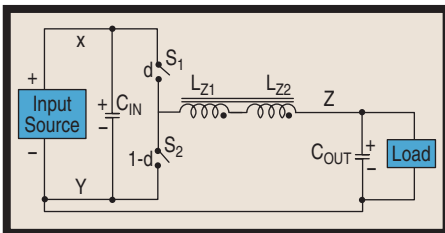


Fig. 3b. Synthesis process: with the output choke split into two separate series connected windings.

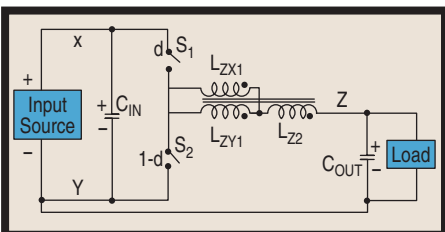


Fig. 3c. Synthesis process: with the new series winding split into two separate parallel connected windings.

No one makes better tantalum capacitors and inductors.



NEC TOKIN Tantalum Capacitors



NEC TOKIN SMD Chip Inductors

Innovation, performance, product quality and reliability. NEC TOKIN is the first and the best.

We introduced the world's first tantalum capacitors in 1955. We led the way in innovation and development. Now we offer you some of the smallest lead-free, large-capacitance capacitors for your high density, high frequency applications. Our power inductors feature some of the lowest profiles and best performance characteristics of the industry in a large selection of inductance values. You can rely on us, because **we make your components from our own raw materials.** Contact us now to receive the latest NEC TOKIN catalog.

NEC / TOKIN

www.nec-tokinamerica.com

Devices thru Material Innovation

NEC TOKIN America, Inc.

UNION CITY, CA / SAN DIEGO, CA / CHICAGO, IL / TAMPA, FL

32950 Alvarado-Niles Rd., Suite 500

Union City, CA 94587

Tel: 510-324-4110 Fax: 510-324-1762

NEC TOKIN Corporation

Global Sales Headquarters: Tokyo, Japan

Tel: 81-3-3402-6179 or visit www.nec-tokin.com

Offices in Germany, UK, Hong Kong, Shenzhen, Shanghai,

Taipei, Singapore, Malaysia, Bangkok, and Seoul

CIRCLE 219 on Reader Service Card

freeproductinfo.net/pet

In Fig. 3(d), we disconnect the two parallel windings at their undotted terminals. In the Fig. 3(d) circuit the coupled inductor is akin to a flyback transformer and the high loop contains the windings, L_{ZX1} and L_{ZY1} .

Key Point No. 4: A series combination of circuit elements can be arranged in any order with no effect on circuit performance provided that the polarities of components are pre-

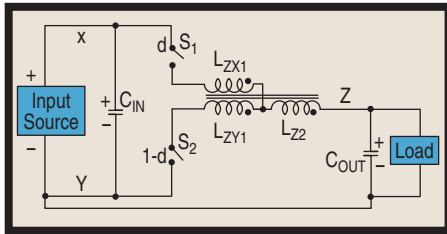


Fig.3d. Synthesis process: with the parallel windings disconnected at the undotted terminals.

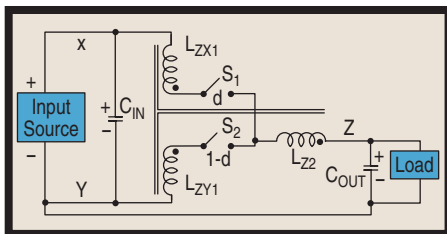


Fig.3e. Synthesis process: with the positions of series connected switches and windings reversed.

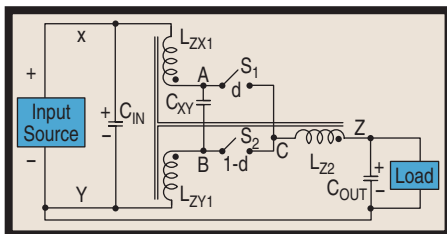


Fig. 3f. Synthesis process: with a capacitor connecting the dotted terminals of the X and Y terminal windings.

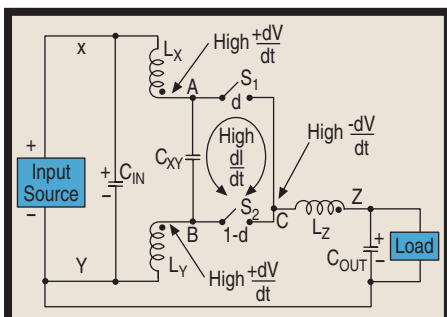


Fig.3g. Synthesis process: with the windings uncoupled from each other.

served if their positions are changed.

Key point No. 4 suggests that we can reverse the positions of switches and windings that are series connected in Fig. 3(d), as illustrated in Fig. 3(e).

Key Point No. 5: The time average voltage across a winding of a transformer or inductor is zero.

Key Point No. 6: If a transformer or coupled inductor has two windings with the same number of turns for which there is a constant dc voltage difference between the undotted terminals of the windings, then a capacitor can be connected between the dotted terminals of the windings and the dc applied voltage to the capacitor will be equal to the dc difference voltage between the undotted terminals. The capacitor will be a preferred path for ac currents, so that by adding the capacitor the ac currents in the two windings will be reduced.

Key point No. 6 suggests that we can connect a capacitor, C_{XY} , as illustrated in Fig. 3(f), between the dotted terminals of the L_{ZX1} and L_{ZY1} windings. Key point No. 5 suggests that the dc applied voltage to capacitor C_{XY} will be equal to the input dc source voltage. Capacitor C_{XY} provides a preferred path for ac pulsating switch currents, so that the L_{ZX1} and L_{ZY1} windings are no longer in the high di/dt loop. The L_{ZX1} and L_{ZY1} windings are the preferred paths for dc currents, so that the L_{ZX1} and L_{ZY1} winding currents are nonpulsating. The circuit of Fig. 3(f) achieves nonpulsating terminal currents at all three terminals, so that voltage spikes generated at the input capacitor in Fig. 1 are eliminated for Fig. 3(f).

Circuits with nonpulsating terminal currents have been known for some time, but the Fig. 3(f) circuit provides an additional benefit, much reduced common mode noise. Fig. 3(g) illustrates the Fig. 3(f) circuit without the magnetic coupling be-

tween windings. With the windings uncoupled the inductors can be any size and value desired. The major noise sources are illustrated in Fig. 3(g).

There are now three circuit nodes with high dV/dt , nodes A, B, and C, however, the wave form at node C is 180° out of phase from the waveforms at nodes A and B. Also, the magnitudes at all the nodes are much less than in the case of the Fig. 1 circuit. We can assume that the windings are magnetically coupled and each of the windings have the same number of turns. Then, with switch S_1 on, the voltage at node A will be half way between the X terminal voltage and the Z terminal voltage, as illustrated in Fig. 4(a). Therefore, the voltage at node A will be:

$$\frac{1}{2} \times (V_X + V_Z) \tag{5}$$

Where:

V_X = X terminal voltage

V_Z = Z terminal voltage.

With switch S_1 off and switch S_2 on, the voltage at node B will be half way between the Z terminal voltage and the Y terminal voltage:

$$\frac{1}{2} \times (V_Z + V_Y) \tag{6}$$

Where:

V_Y = Y terminal voltage

The node A voltage will be equal to the node B voltage plus the capacitor C_{XY} voltage which is just the input voltage. Hence, the voltage swing for the node A is: (see Equation 7, below)

Where:

ΔV_A = Voltage swing of node A in Fig. 3(f)

The voltage swing for node A in Fig. 3(f) is half of the voltage swing of node A in the Fig. 1 circuit and rate of voltage rise or fall for Fig. 3(f) is:

$$\frac{dV_A}{dt} = \frac{V_I}{2 \times T_{TR}} \tag{8}$$

Since node B is capacitively coupled to node A, the voltage swing for node

$$\Delta V_A = [(V_X - V_Y) + \frac{1}{2} \times (V_Z + V_Y)] - \frac{1}{2} \times (V_X + V_Z) = \frac{1}{2} \times (V_X - V_Y) = \frac{1}{2} \times V_I$$

Equation 7.

B will be equal to the voltage swing for node A. Node C has a voltage swing equal in magnitude to the voltage swing for nodes A and B, but the wave form at node C is 180° out of phase, so that common mode current from the node C cancels common mode

current from nodes A and B and:

$$\frac{dV_C}{dt} = \frac{-V_I}{2 \times T_{TR}} \quad (9)$$

Compare Fig. 2(e) with Figs. 4(a), 4(b) and 4(c). The amount of cancellation depends on the parasitic capacitance associated with the nodes. If nodes A and B have higher parasitic capacitance than node C then we can add a neutralizing capacitor(s) or we can adjust the turns ratio between the Z terminal winding and the X and Y terminal windings to achieve complete cancellation. If the windings are coupled, the X and Y terminal windings must have equal turns.

By increasing the Z winding turns with respect to the X and Y winding turns, the voltage swing at node C increases in magnitude and the voltage swings at nodes A and B decrease in magnitude. The ratio of the Z winding turns to the X and Y winding turns can be adjusted to achieve the maximum amount of common mode noise cancellation.

Fig. 5 is a summary outline of the synthesis method introduced here. The outline suggests that the synthesis method is applicable to any three terminal network with a winding in series with the Z terminal of the three terminal network. The synthesis method is applicable, in general, to any three terminal network of the type

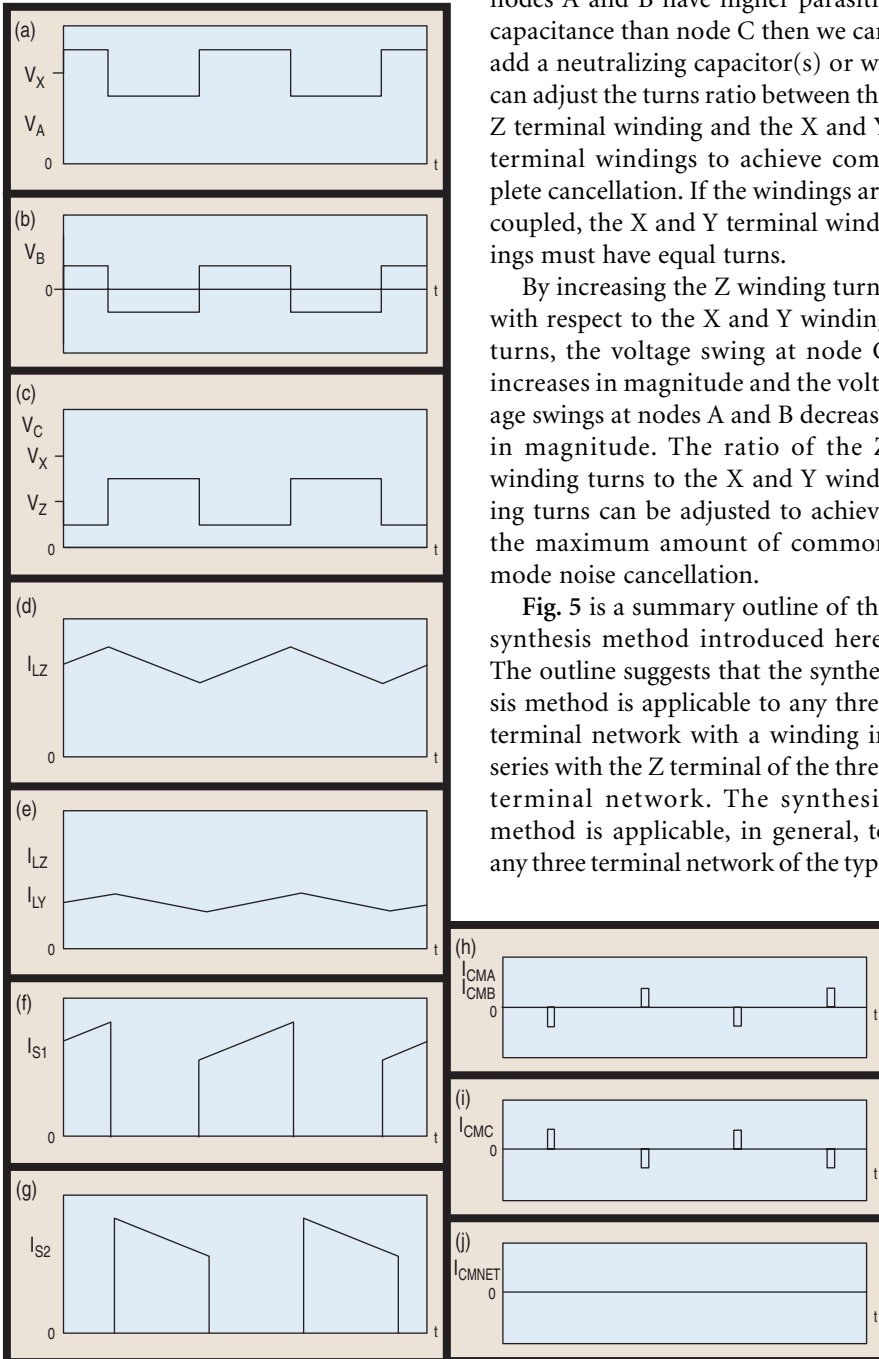


Fig. 4. Wave forms of the fig.3(f) circuit, (a) node A voltage, (b) node B voltage, (c) node C voltage, (d) Z winding current, (e) X and Y winding currents, (f) S_1 switch current, (g) S_2 switch current, (h) common mode noise current generated by nodes A and B, (i) common mode noise current generated by node C, (j) total net common mode noise current from nodes A, B, and C.

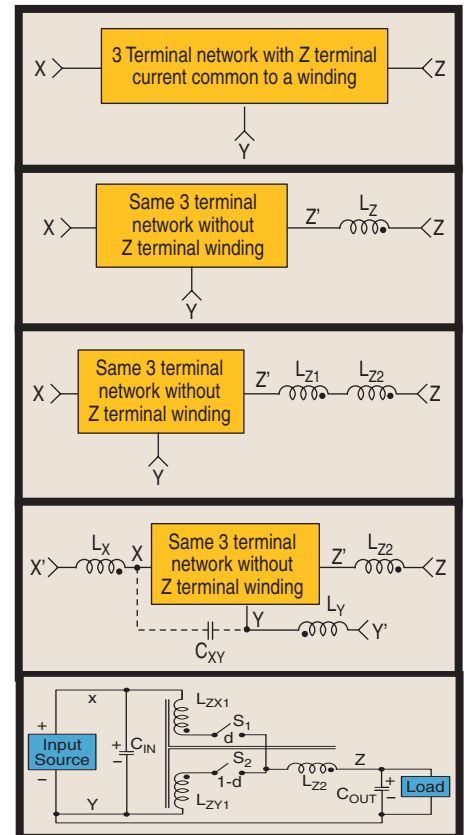


Fig. 5. A generalized synthesis method for transforming a three terminal network with a winding network connected in series with the Z terminal to a new three terminal network with improved terminal current properties, improved ac performance, and improved common mode noise performance.

indicated and, although Fig. 5 illustrates the synthesis method for a single winding in series with the Z terminal, the method applies to winding networks in series with the Z terminal. In Part 2 of this series, we'll show how the synthesis method can be simply extended to achieve three terminal networks with zero ripple for all three terminals, what might be considered a true near-zero emissions topology. The reference below describes and illustrates some of the new circuits we will be describing. **PETech**

References

Wittenbreder, E.H., "Power Electronic Circuits With All Terminal Currents Non-Pulsating," US Patent 6,304,065.

For more information on this article, CIRCLE 333 on Reader Service Card