

Part One

Forward-Converter Design Leverages Clever Magnetics

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A synchronous rectified forward converter optimized for performance and cost uses coupled inductors for output filtering and transformer-based gate drive.

Digital signal processing ICs continue to demand more current and power as their voltage requirements drop. In applications such as consumer electronics, achieving high efficiency while designing for the lowest possible cost can be daunting for design engineers. One solution to this apparent paradox is a power supply for a consumer application that uses a two-output 130-W forward converter with synchronous rectification as well as a coupled-output inductor. With this method, a downstream dc-dc converter can then step down the output voltage from the forward converter to achieve levels consistent with the needs of the signal-processing ICs.

In part one of this two-part article, design requirements for the forward converter are defined and topology selection is explained. Procedures are then given for designing the input rectifier filter and the transformer. In part two, which will appear in the August 2007 issue, the design of the coupled-output inductor and the selection of the synchronous MOSFETs and output capacitors are described. This section will also discuss requirements for loop compensation and present results for the final design

Synchronous Rectification

One method to increase efficiency in a power supply with a forward converter is to employ synchronous rectification. Synchronous rectification involves using MOSFETs instead of standard or Schottky diodes as output rectifiers. Rectifier loss drops dramatically, particularly with low-voltage outputs, when using MOSFETs as opposed to diodes. This is because the conduction loss of the MOSFET ($R_{DS(ON)} \times I_{DS}^2$) is lower than the diode loss of ($V_{DIODE} \times I_{DIODE}$). There are secondary-side controllers that can control the turn on and turn off of the MOSFETs. However, the MOSFETs also can be self-driven directly from the transformer. This is the more cost-effective approach that will be used in this design.

| Output voltage (V) | Output current (A) | Output power (W) |
|--------------------|--------------------|------------------|
| 3.3 | 9.50 | 32.5 |
| 5 | 7.25 | 36.25 |
| 7 | 1.6 | 11.2 |
| 12 | 3.75 | 45 |

Table 1. Output ranges for set-top box power supply.

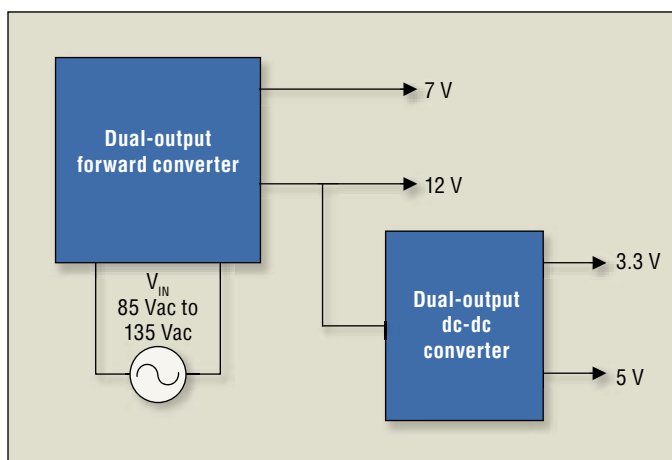


Fig. 1. This architecture for a high-end set-top box power converter is designed for units operating in the United States.

Input/Output Requirements

The power supply in our example was designed for a consumer application, specifically a high-end set-top box. The set-top box was designed for use in the United States. Consequently, the input-voltage range was specified to be 85 Vac to 135 Vac. The output voltages are summarized in Table 1.

To achieve tight regulation and high efficiency, a downstream dual-output dc-dc converter was used to generate both 5 V and 3.3 V. The input voltage will be 12 V, which is the

| Forward-converter output voltage (V) | Forward converter without downstream dual-output dc-dc converter | | Forward converter with downstream dual-output dc-dc converter | |
|--------------------------------------|--|------------------------------------|---|------------------------------------|
| | Forward-converter output current (A) | Forward-converter output power (W) | Forward-converter output current (A) | Forward-converter output power (W) |
| 12 | 3.65 | 45 | 10.0 | 120 |

Table 2. Forward-converter power requirements.

main output from the forward converter. A secondary output from the forward converter would generate 7 V. A block diagram for the complete converter is shown in Fig. 1.

The feedback loop for the forward converter will be closed around the 12 V output. Using 12 V as the input rail to the dc-dc converter will increase the current, and therefore the power demand on the 12-V supply, according to the data listed in Table 2. The projection of increased power was based on an assumption that the efficiency of the dc-dc converter is 90%. Although the design of the 5-V/3.3-V dc-dc converter is certainly an interesting exercise, the focus here will be on the design of the forward converter.

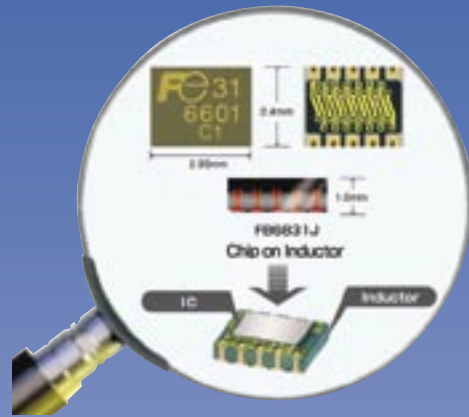
Initial Considerations

After the input and output specifications are determined, as well as any other important requirements, the next step is to decide on the topology to be used. Although a flyback converter could be made to work in this application, a forward converter might be a better choice — especially considering cost — in applications where the output voltages are low and output currents are high. One reason is that the ripple currents in the output capacitors are significantly lower for a forward converter than, for example, a comparable discontinuous-mode flyback converter. Lower capacitor ripple currents translate into smaller and fewer output capacitors, which reduces costs.

Once the topology is selected, the design engineer must decide on a controller. For this design, Fairchild Semiconductor's FS7M0880 is used. This fixed-frequency current-mode PWM controller integrates an 8-A, 800-V switching FET device. Having the FET incorporated in the same IC as the controller eliminates components, which, again, helps to reduce cost and increase reliability. The device's frequency is internally set to 66 kHz. The duty cycle is clamped to a typical value of 50%, which is important in the design of a forward converter (to be discussed in further detail later). This controller also contains all the necessary protection functions, including pulse-by-pulse current limiting, overload protection, overvoltage protection (OVP) and soft-start.

Having decided on a forward converter and a controller, the next step is to choose a transformer-reset scheme. Recall that a forward converter needs a method by which to reset the magnetic flux in the transformer back to zero after each on period, otherwise the transformer will drift into

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V_{in}=2.7V-5.5V, V_{out} min=0.8V,
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Switching frequency=2.5MHz

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- Integrated controller, FETs and inductor
- IC chip on inductor structure
- Inductor with terminal pins

- **Advantages**

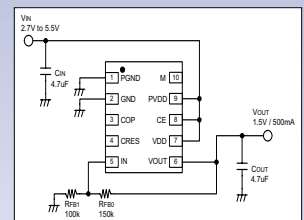
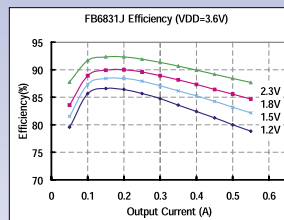
- Reduced size/weight
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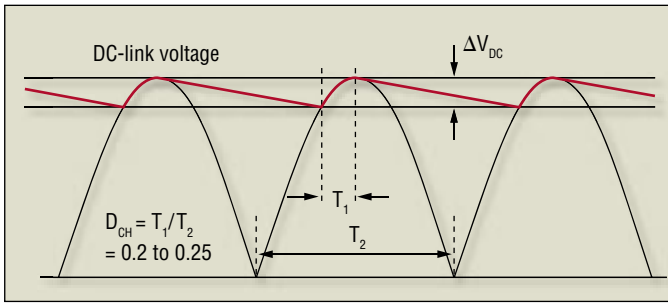


Fig. 2. The waveform for the dc-link voltage on the output of the bridge rectifier illustrates how the holdup capacitance of the filter capacitor is carefully sized to have a specific charge duty cycle, D_{CH} [1].

saturation after several cycles. The choices for reset include the traditional options of reset winding, resistor, capacitor, diode (RCD) reset, or an active clamp. Each option has its own set of advantages and disadvantages. The active-clamp approach generally requires a controller capable of supporting active-clamp operation. With the RCD approach, power will be dissipated in the resistor and will adversely affect overall efficiency. Therefore, the traditional reset winding was chosen for this design.

Input-Rectifier Filter Design

The first step in the design process is to address the input ac-dc input-conversion circuitry, specifically the bridge rectifier and filter capacitor. In this case, a standard bridge rectifier and electrolytic-filter capacitor arrangement will be used. The value of the input-filter capacitor impacts subsequent calculations regarding the transformer. Since this forward converter will have two outputs, the delivered output power is easily calculated using Eq. 1:

$$P_O = (V_{OUT(12V)} \times I_{OUT(12V)}) + (V_{OUT(7V)} \times I_{OUT(7V)}) = (12 \text{ V} \times 10 \text{ A}) + (7 \text{ V} \times 1.6 \text{ A}) = 131.2 \text{ W.} \quad \text{Eq. 1}$$

Using a goal of 85% efficiency, for the forward converter, the input power can be calculated using Eq. 2:

$$P_{IN} = \frac{P_O}{\eta} = \frac{131.2}{.85} = 154.4 \text{ W.} \quad \text{Eq. 2}$$

There is a widely accepted rule of thumb regarding the sizing of the input electrolytic capacitor when operating across the range of ac mains voltages within the United States. This is to allow a capacitance per load of 2 $\mu\text{F}/\text{W}$ to 3 $\mu\text{F}/\text{W}$. In this case, a 470- μF capacitor can be used. However, if a specific holdup time must be met, then that value may change. In this design, a 680- μF capacitor is used in this design. Based on this value, the ripple voltage can be calculated using Eq. 3:

$$\Delta V_{DC} = \frac{P_{IN} \times (1 - D_{ch})}{\sqrt{2} \times V_{AC(MIN)} \times 2 \times f_L \times C_{DC}}, \quad \text{Eq. 3}$$

where C_{DC} is the value of the electrolytic-filter capacitor, f_L is ac-line frequency, $V_{AC(MIN)}$ is the minimum ac-line voltage and D_{CH} is the capacitor charging duty cycle (a typical value is 0.2). The capacitor charging duty cycle is illustrated in Fig.

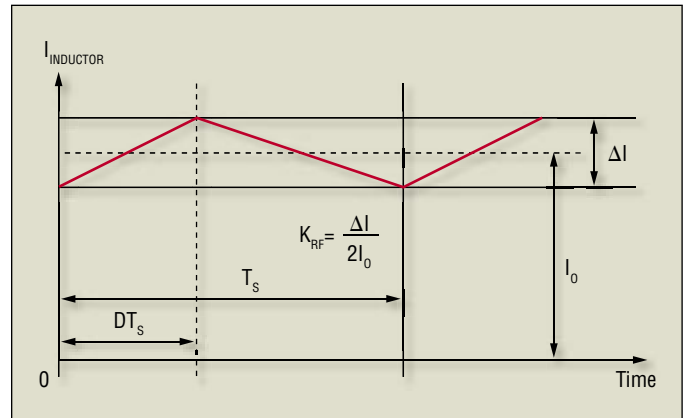


Fig. 3. The ripple-current factor K_{RF} affects several aspects of the converter and must be established early in the design process. It is typically assigned a value between 0.1 and 0.2 [2].

2. Substituting the appropriate values in Eq. 3 yields a ripple voltage of $\Delta V_{DC} = 13 \text{ V}$. Subtracting this value from the peak voltage at minimum ac-line voltage yields the minimum dc voltage in Eq. 4:

$$V_{DC(MIN)} = \sqrt{2} \times V_{AC(MIN)} - \Delta V_{DC} = \sqrt{2} \times 85 - 13 = 107 \text{ V.} \quad \text{Eq. 4}$$

The maximum dc-link voltage is calculated assuming there is no load on the filter capacitor at the maximum ac-line voltage. This can be determined by Eq. 5:

$$V_{DC(MAX)} = \sqrt{2} \times V_{AC(MAX)}. \quad \text{Eq. 5}$$

Primary-Side Calculations

As mentioned previously, the method for transformer reset will be the traditional, separate reset-winding approach. While looking at the specification for the FS7M0880, note that although the maximum duty cycle is typically 50%, it can vary from 45% to 55%. This variation slightly complicates the design in that the power-handling capability must be calculated at 45% duty cycle, whereas the turns ratio for the reset winding must be calculated for the maximum duty cycle of 55%.

Recall that duty cycles larger than 50% are allowable in a single-switch forward converter, provided that the reset winding turn count is reduced accordingly to allow the core to be reset in a shorter period of time. The penalty for this will be increased voltage across the FET during off time. However, since the controller uses an 800-V FET, increased voltage will not be a problem in this application. By using inductor volt-second balance to the transformer-magnetizing inductance, it can be shown that:

$$D_{MAX} \leq \frac{1}{1 + \frac{N_{RESET}}{N_{PRI}}}. \quad \text{Eq. 6}$$

Typically, if the duty cycle is clamped to 50%, then the turns ratio of the reset winding to the primary winding will be 1:1. However, since the controller duty cycle could conceivably reach 55%, then Eq. 7 can be algebraically manipulated to solve for the turns ratio for that condition:

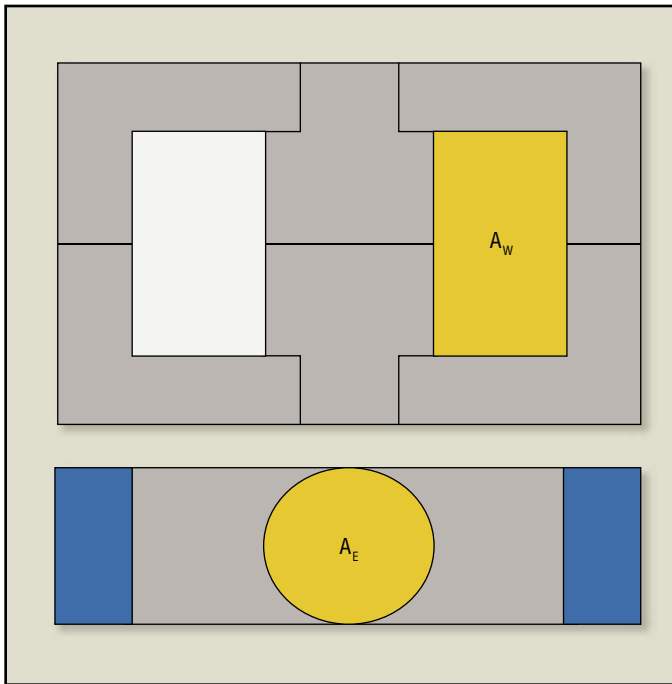


Fig. 4. The area product of a transformer is the product of the window-winding area, A_w and the cross-sectional area of the core, A_e [3].

$$\frac{N_{\text{RESET}}}{N_{\text{PRI}}} = \frac{1 - D_{\text{MAX}}}{D_{\text{MAX}}} = \frac{1 - .55}{.55} = 0.82. \quad \text{Eq. 7}$$

Eq. 8 is used to determine the voltage stress across the FET during off time. Using the previously calculated values for $V_{\text{DC(MAX)}}$ and $N_{\text{PRI}}/N_{\text{RESET}}$, the expected maximum drain-source voltage across the FET can be calculated as listed in Eq. 8:

$$V_{\text{DS(MAX)}} = V_{\text{DC(MAX)}} \times \left(1 + \frac{N_{\text{PRI}}}{N_{\text{RESET}}}\right) = 190.89 \text{ V} \times \left(1 + \frac{1}{0.82}\right) = 423.7 \text{ V}. \quad \text{Eq. 8}$$

Although the drain-source voltage is higher than it would be if the primary-to-reset winding turns ratio was 1:1 ($V_{\text{DC(MAX)}} = 2 \text{ V}$), there is still plenty of guard band with the FS7M0880.

The next step is to decide on the ripple-current factor in the output inductor, as this impacts several subsequent calculations. The relationship of the ripple factor to other parameters of the inductor-current waveform is shown in Fig. 3. Mathematically, the ripple factor is described in Eq. 9 as the ratio of the peak-to-peak inductor-ripple current to twice the dc-output current:

$$K_{\text{RF}} = \frac{\Delta I}{2 \times I_{\text{O}}}. \quad \text{Eq. 9}$$

Making the ripple factor smaller will reduce the ripple current in the inductor; however, it will also make for a larger inductor. A typical rule of thumb is to set K_{RF} between 0.1 and 0.2. In this design a value of 0.15 for K_{RF} is used. Now the peak current in the FET can be calculated using Eq. 10:

$$I_{\text{DS(PEAK)}} = \frac{P_{\text{IN}}}{V_{\text{DC(MIN)}} \times D_{\text{MAX}}} \times (1 + K_{\text{RF}}). \quad \text{Eq. 10}$$

The factor of $P_{\text{IN}}/(V_{\text{DC(MIN)}} \times D_{\text{MAX}})$ represents the average transistor current during the transistor's on time, which we will label as I_{EDC} . It is important to emphasize that because peak current deals with power processing (as opposed to resetting the transformer), the lowest maximum duty cycle available from the FS7M0880, which is 45%, must be used. This leads to a value of 3.71 A for $I_{\text{DS(PEAK)}}$. This number needs to be compared to the current-limit trip point of the FS7M0880 in order to make sure normal operation will not cause a nuisance shutdown. The datasheet shows that the minimum trip point is 4.4 A, which has the appropriate margin. The rms current through the FET also needs to be calculated. This rms current defined in Eq. 11 also will be used later in the transformer calculations:

$$I_{\text{DS(RMS)}} = I_{\text{EDC}} \times \sqrt{(3 + K_{\text{RF}}^2) \times \frac{D_{\text{MAX}}}{3}} = \frac{154.4 \text{ W}}{(107 \text{ V} \times 0.45)} \times \sqrt{(3 + 0.15^2) \times \frac{0.45}{3}} = 2.16 \text{ A}. \quad \text{Eq. 11}$$

Transformer Design

The next step in the design procedure is the transformer design. First, the area product should be calculated. The area product is the cross-sectional core area of the transformer multiplied by the winding window area. Fig. 4 shows the cross-sectional area of the core, A_e , and the window area, A_w . This number can then be taken to core manufacturers' data books to determine the proper core. Eq. 12 shows the mathematical expression for area product. The term 10^4 is included so the equation produces a number expressed in units of mm^4 . The term ΔB represents the flux-density swing in Teslas:

$$AP(\text{in } \text{mm}^4) = A_e \times A_w = \left(\frac{78.72 \times P_{\text{IN}}}{\Delta B \times f_{\text{SW}}}\right)^{1.31} \times 10^4. \quad \text{Eq. 12}$$

This formula applies to a forward converter. The result will be a rough estimate of the transformer core size required to process the required power. However, other factors, such as pin count and winding length of the bobbin, can come into play, as they do for this design. For example, using the previously calculated value for P_{IN} and a relatively conservative value of 0.22 T for ΔB , the AP is calculated as 8053 mm^4 . According to the TDK data book, the EER28 or EER28L cores would appear to be adequate based on their area products. However, subsequent calculations would show that an EER35 would require fewer turns, and the longer winding length would allow for single layers for the primary and secondary windings. Therefore, the EER35 transformer core is used in this design.

The EER35 has a cross-sectional area of 107 mm^2 . The next step is to calculate the minimum primary-turns count using Eq. 13.

| Winding stack position | Thickness (mm) | Winding description | Number of turns | Number of wires | Wire gauge (AWG #) |
|--|----------------|---|-----------------|-----------------|--------------------|
| 6 | 5.0 | V _{CC} | 3 | 1 | 24 |
| 5 | 3.0 | Primary, 2 nd half | 16 | 2 | 23 |
| 4 (Three windings share this position.) | 5.0 | Gate drive (high side) / Output (7 V) / Gate drive (low side) | 3 / 5 / 3 | 1 / 2 / 1 | 24 / 23 / 24 |
| 3 | 3.0 | Output (12 V) | 8 | 3 | 21 |
| 2 | 3.0 | Primary, 1 st half | 16 | 2 | 23 |
| 1 | 2.5 | Reset | 26 | 1 | 21 |

Table 3. Winding stack up for forward-converter transformer with EER35 core and 12-pin bobbin.

$$N_{PRI(MIN)} = \frac{V_{DC(MIN)} \times D_{MAX}}{A_E \times f_{SW} \times \Delta B} \times 10^6 = \frac{107 \text{ V} \times 0.45}{107 \text{ mm}^2 \times 66 \text{ kHz} \times 0.22 \text{ T}} \times 10^6 \approx 31$$

Eq. 13

Since this is a minimum number, rounding up yields 32 turns. As an even number, this value can simplify the task of determining the turn counts for the other windings that are based on the primary turns count. The reset winding was determined earlier to be $(0.82) \times N_{PRI}$, or 26 turns. The 12-V winding turns count can be determined by Eq. 14:

$$N_{WINDING(12V)} = \frac{N_{PRI} \times (V_{OUT(12V)} + V_{DIODE(12V)})}{V_{DC(MIN)} \times D_{MAX}}$$

Eq. 14

$V_{OUT(12V)}$ and $V_{DIODE(12V)}$ represent the 12-V supply and the associated rectifier drop. Using synchronous rectification, the forward-conduction voltage drop will depend on the $R_{DS(ON)}$ of the FET used. For now, assume a voltage drop of 0.2 V, in which case the 12-V winding will be eight turns. A similar approach can be used to determine the 7-V winding turns count. However, Schottky diodes will be used in the 7-V supply, as the output current is not high enough to justify the use of synchronous rectification. This yields a 7-V winding turns count of five turns.

Note that the V_{CC} winding is out of phase with output windings. Keep in mind that in a forward converter, an output inductor is required for each winding. This requirement can be alleviated if the winding is out of phase. Remember that the out-of-phase winding will be essentially unregu-

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lated, and in this case, the V_{CC} voltage will vary with the ac-line voltage. Therefore, V_{CC} is proportional to the reset winding rather than the primary. To calculate the V_{CC} turns count, Eq. 15 should be used:

$$N_{VCC} = \frac{N_{RESET} \times (V_{VCC} + V_{DIODE(VCC)})}{V_{DC(MIN)}} \quad \text{Eq. 15}$$

It should be noted that Eq. 15 produces a value of 3.8 turns for the V_{CC} turns count, which rounds up to 4 turns. Yet after building the supply, it was noticed that the V_{CC} voltage was running somewhat high due to the light load on the winding. The V_{CC} voltage was even approaching the OVP trip point of the FS7M0880 controller. Consequently, a single turn was removed from that winding to provide more OVP margin.

The synchronous-drive windings must be calculated carefully so that the gate-source voltages are high enough for driving the gates of the FETs, yet low enough to prevent overstressing them. Looking at the schematic, it will be noticed that the high-side output FET will be on when the primary switch is on. Conversely, the low-side FET will be on during the primary-side FET's off time. Consequently, the high-side gate-drive voltage is inversely proportional to the primary turns count, whereas the low-side gate drive is related to the turns count of the reset winding. The gate-source voltage should be calculated at both high- and low-line conditions, while the FET is both on and off. This ensures the gate-drive voltage is sufficient to drive the FET without the risk of breakdown.

In this design, three turns are used for each gate-drive winding. This is summarized in the following equations for the high-side drive (Eq. 16) and low-side drive (Eq. 17):

$$V_{GS(HS)} = \frac{N_{GS} \times V_{DC}}{N_{PRI}} \quad \text{Eq. 16}$$

$$V_{GS(LS)} = \frac{N_{GS} \times V_{DC}}{N_{RESET}} \quad \text{Eq. 17}$$

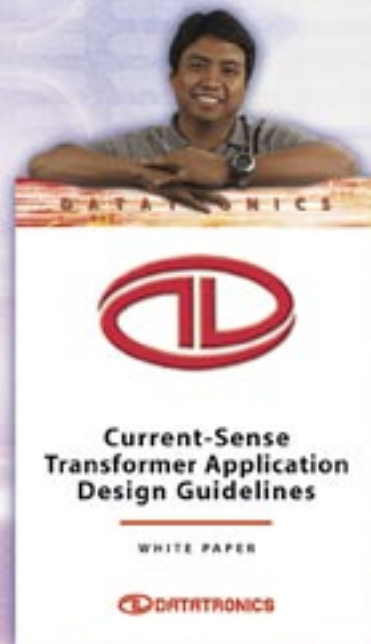
When calculating wire size for the secondary windings, the first point to consider is the current density. A rule of thumb is to keep the current density below 5 A/mm² (395 circular mils/Amp). It is not necessary, but desirable to keep the windings to single layers that span the bobbin width minus the required margins on each side. Single layers tend to reduce eddy-current losses when compared to multiple layers. Coupling between the windings also can be improved with single-layer windings. Splitting the primary winding into two series windings, and then sandwiching the secondary windings between them also will improve the coupling, and therefore reduce the leakage inductance. A drawing of the winding stack up for this transformer design is shown in Table 3. **PETech**

References

1. Choi, Hang-Seok, Fairchild Semiconductor, Application Note AN4134, p. 2, March 24, 2004
2. Choi, Hang-Seok, Fairchild Semiconductor, Application Note AN4134, p. 3, March 24, 2004
3. Choi, Hang-Seok, Fairchild Semiconductor, Application Note AN4134, p. 4, March 24, 2004

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