

Active Clamp Resets Transformer in Converters

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Active clamp technique is employed to reset the transformer in a forward converter topology. In addition, active clamp is shown to improve power-conversion efficiency.

Power converters based on the forward topology offer high efficiency and good power-handling capability in applications up to several hundred watts. The operation of the transformer in a forward topology doesn't inherently self-reset each power switching cycle as do push-pull, half-bridge and full-bridge power converters. The transformer in a forward converter requires the application of a mechanism to reset the transformer each power cycle. Several different reset mechanisms have been employed, each with their own benefits and challenges. The active clamp reset mechanism is presently finding extensive use in medium-level power converters in the 50-W to 200-W range.

The forward topology has been widely used for decades. Its popularity has been based on many factors, such as positive cost, complexity and efficiency tradeoffs. The forward converter is derived from the buck topology family,

employing a single modulating power switch. The power switch for the forward topology is ground referenced, whereas in the buck topology, the switch source floats on the switching node. The main difference between the topologies is that the forward topology employs a transformer to provide input/output ground isolation and a step-down or step-up function. Fig. 1 shows the similarities between a buck and forward converter. Note the only difference between the transfer functions is the inclusion of the transformer term (N_s/N_p) in the forward transfer function. N_s and N_p are the number of secondary and primary wire turns respectively wound on the transformer.

Fig. 2 presents a more detailed look at a transformer used in a forward power converter. Note the "magnetizing inductance" (L_m) shown in parallel with the primary winding. This magnetizing inductance can be measured at

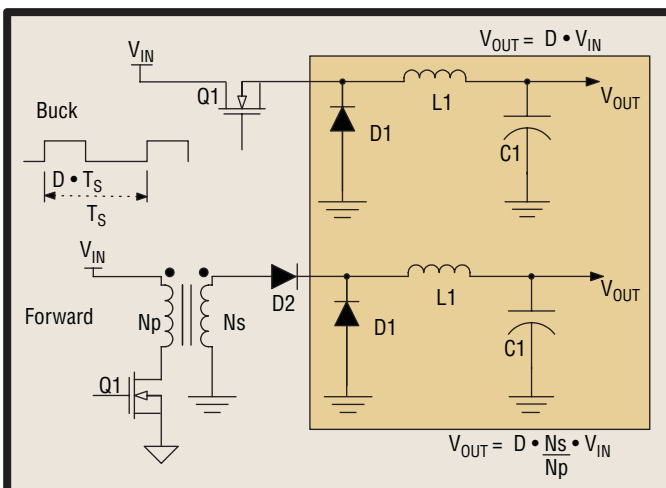


Fig. 1. Buck and forward topology.

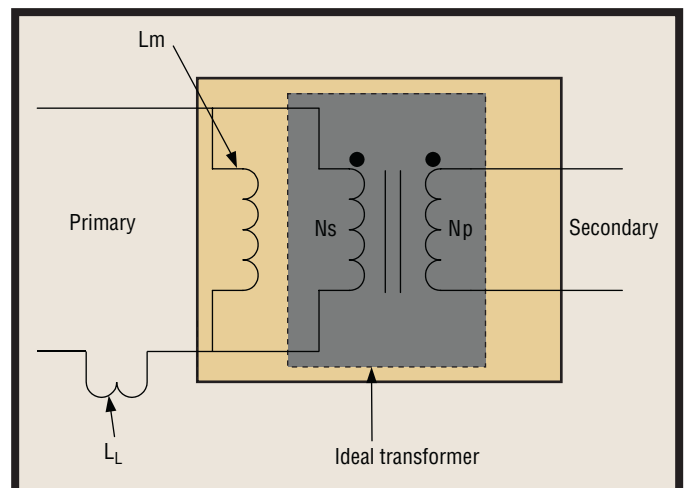


Fig. 2. Transformer model.

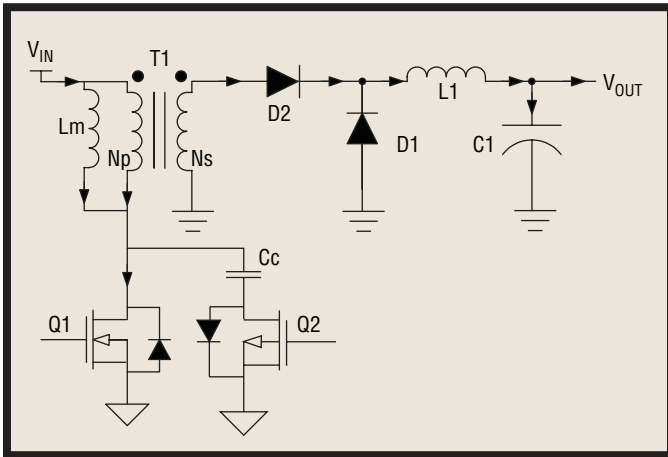


Fig. 3a. Operation at step t0.

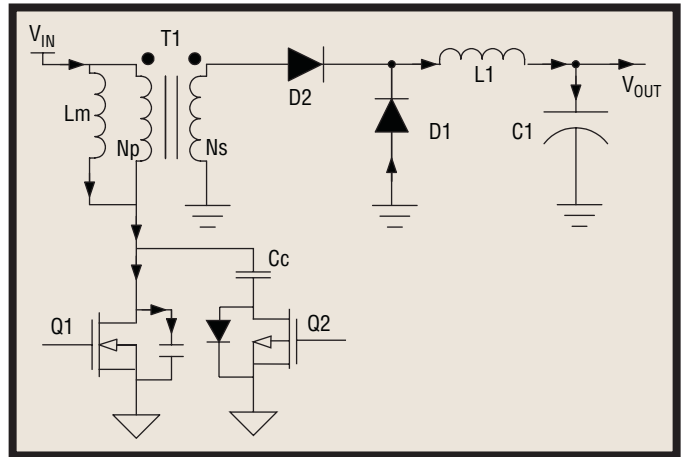


Fig. 3b. Operation at step t1.

the primary terminals with the secondary winding(s) open circuit. The peak current in the magnetizing inductance is proportional to the maximum flux density within the core. A given-size core can only handle a limited flux density before saturation of the core occurs. At core saturation, a rapid reduction of inductance occurs.

The other element added to the transformer model is a “leakage inductance” term in series with the primary winding; this leakage inductance can be measured at the primary terminals with the secondary winding(s) short-circuited. This term represents the stray primary inductance, which doesn’t couple primary to secondary. With careful design, the value of this inductance can be kept rather small and the effect on the power converter limited to voltage spikes on the power switch.

Circuit Operation

Figs. 3a-3f illustrate the six operational steps of a forward power converter. At time t0, the main power switch (Q1) is on, applying V_{IN} across the transformer primary. The transformer secondary winding voltage is $V_{IN} \times N_s/N_p$. The primary current is comprised of two components at this time: the reflected current from the output inductor ($I_L \times N_s/N_p$) and a current ramping up in the magnetizing inductance (L_m). The reset switch Q2 is open, and the clamp capacitor (C_c) has been previously charged to a voltage of $V_{IN}/(1-D)$, which we’ll explain later. This step of the cycle is the power phase, as energy is being transferred to the secondary during this step. The first order duration of this step is $T_s \times V_{OUT}/V_{IN}$, where T_s is the switching period.

At time t1, the main power switch is turned off, completing the power step. The magnetizing current continues to flow. However, rather than flowing into the MOSFET channel, the current flows into the drain-to-source capacitance. The drain-to-source capacitance linearly charges

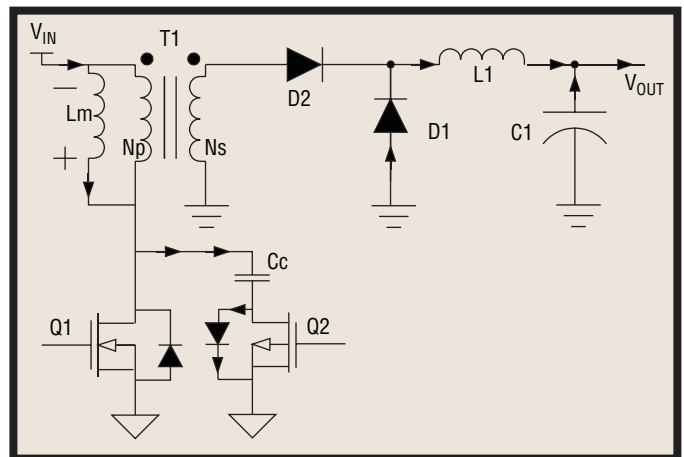


Fig. 3c. Operation at step t2.

up to the same potential as the clamp capacitor (C_c). The clamp capacitor voltage is greater than V_{IN} , so at this time, the voltage across the transformer primary is re-versed, compared to the power step of t0. If the main switch is quickly turned off prior to any appreciable increase in the drain voltage, the resulting switching losses will be very low because the channel current would have decreased to

With careful design, the value of this inductance can be kept rather small value and the effect on the power converter limited to voltage spikes on the power switch.

zero prior to any drain voltage increase across the switch.

At t2, the drain voltage of the main switch has risen to the clamp capacitor potential. The magnetizing current will now flow through the clamp capacitor and forward bias the body diode of the reset switch (Q2). Because the potential across the magnetizing inductance has been reversed, the magnitude of the magnetizing current will start to decrease.

At t3, the reset switch is turned on. Because the

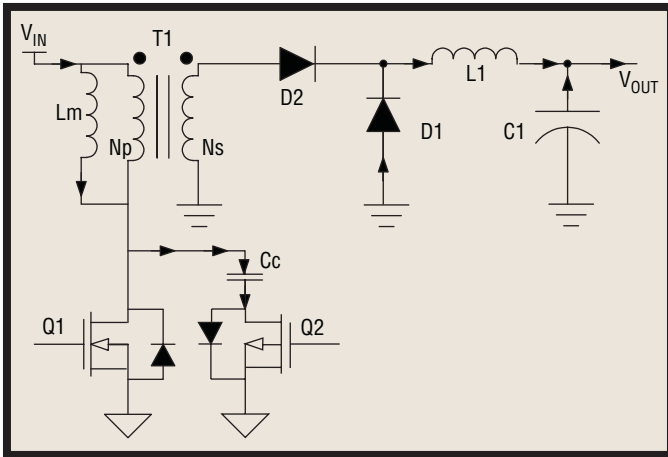


Fig. 3d. Operation at step t_3 .

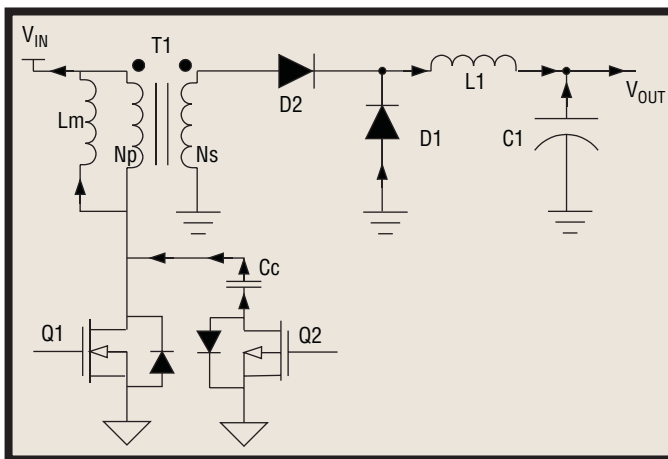


Fig. 3e. Operation at step t_4 .

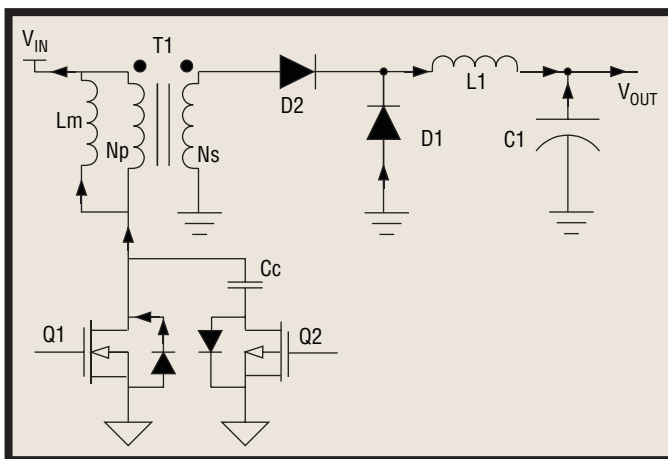


Fig. 3f. Operation at step t_5 .

device's body diode was forward biased and the drain-source potential was approximately zero, this transition has minimal switching losses. As the magnetizing current flows through the reset switch and into the clamp capacitor, the magnitude of current continues to decrease as energy is being transferred from the magnetizing inductance into the clamp capacitor. The voltage

across the clamp capacitor continues to increase and peaks when the magnetizing current reaches zero.

At t_4 , the current in the magnetizing inductance reaches zero and starts to build in the reversed direction sourced from the clamp capacitor through the reset switch, the magnetizing inductance and back to the source (V_{IN}). The current will continue to build in the reversed direction as the clamp capacitor returns the energy that it captured from the magnetizing inductance at the end of the power cycle, t_0 . Steady-state conditions require the clamp capacitor voltage to return to the starting potential and the magnetizing current to have the same magnitude (opposite polarity) at the conclusion of this reset time.

At t_5 , the switching period is complete, as defined by the controller oscillator period. The reset switch is turned off, stopping the flow of current from the clamp capacitor. In steady-state conditions, the clamp capacitor is charged again to a potential of $V_{IN}/(1-D)$. The magnetizing current will discharge the main switch drain-source capacitance until the drain potential equals the input voltage and the voltage across the transformer primary is 0 V.

After a short delay from t_5 , t_6 begins with the main switch turning on again to start a new cycle. The delay is configurable within the LM5025 controller, which should be set so the drain source capacitance of Q1 has sufficient time to discharge to V_{IN} . This helps to reduce switching losses when Q1 turns on.

Fig. 4 shows several of the key circuit waveforms. The uppermost waveforms are the modulator ramp and error signals, which determine the main switch on time. The center waveform is the main switch drain voltage, which is low when the switch is on and rises to the clamp capacitor potential when the switch is off. The dashed line in the lower waveform represents the magnetizing inductance current, which flows through the clamp capacitor (solid line waveform) for the reset time. As expected, both currents are balanced around the zero.

Benefits of Active Clamp Reset

Several switching loss benefits have already been discussed. Of primary concern are turn-on and turn-off losses for the main power switch.

With sufficiently fast gate drive, the turn-off loss of Q1 can be virtually lossless. To accomplish this, the gate of Q1 must be turned off (and the flow of current stopped) before the drain voltage has a chance to rise, which is delayed because of the drain-source capacitance. Using a compound gate driver made up of both MOS and bipolar devices provides a high-peak gate discharge current to ensure a fast turn-off and reduced switching losses. Turn-on losses can be reduced with proper selection of the delay from t_5 to t_6 , allowing time for the drain voltage reduction prior to the initiation of the main switch.

For steady-state conditions, the voltage \times time product applied to the magnetizing inductance, over a complete cycle, must equal zero. When the main switch is on, the volt

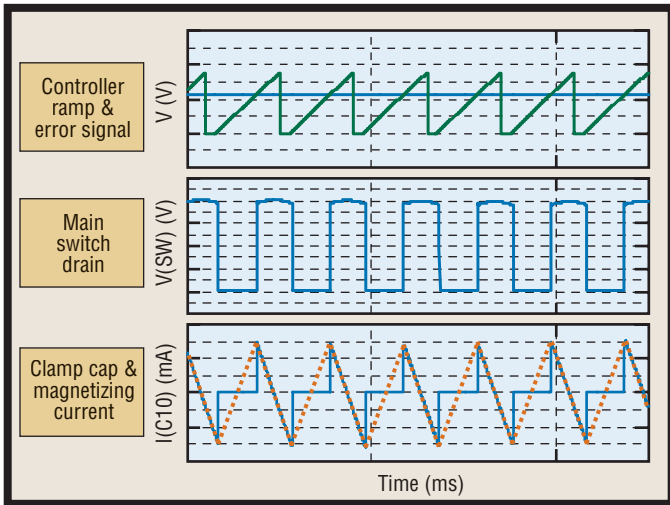


Fig. 4. Key active clamp waveforms.

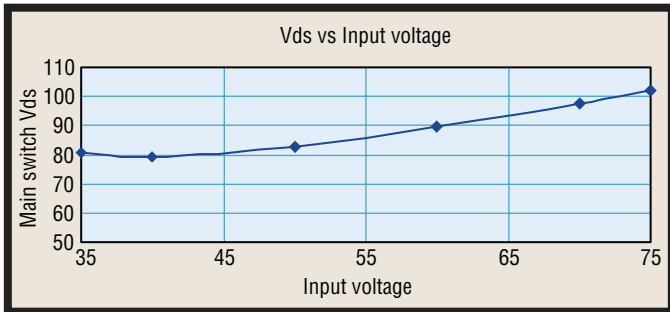


Fig. 5. Main switch V_{DS} vs. V_{IN} .

× time product is $V_{IN} \times D \times T_s$, where D is the on time duty cycle (D) and T_s is the switching period. The off period is defined as $(1-D) \times T_s$. The voltage across the primary when the main switch is off is: $V_C - V_{IN}$. Where V_C is the clamp capacitor voltage. Setting the equality:

$$V_{IN} \times D \times T_s = (V_C - V_{IN}) \times (1-D) \times T_s \text{ solving for } V_C = V_{IN}/(1-D).$$

Remember that D decreases as V_{IN} increases. The clamp capacitor voltage will adapt to changing line (V_{IN}) conditions to maintain this equality. This important feature minimizes the voltage stress across the main switch for all operating conditions, thus allowing use of lower V_{DS} rated devices. A plot of the main switch V_{DS} vs. input voltage (V_{IN}) is shown in Fig. 5. Note that V_{DS} doesn't increase proportionally with V_{IN} . A lower MOSFET V_{DS} rating leads to lower on resistance and lower gate charge, which translates into higher overall efficiency.

Demonstration Results

A schematic diagram of an active clamp-based forward converter is shown in Fig. 6. This design operates over an input voltage range of 36 V to 75 V. The output is rated for up to 100 W at 3.3 V. The power transformer has a 6-to-1 turns ratio. The primary winding is made of 12 turns, and the secondary winding is made of two turns. A planar construction technique is employed. The primary is fabricated with a multi-layer PC board. The high-current secondary is fabricated with

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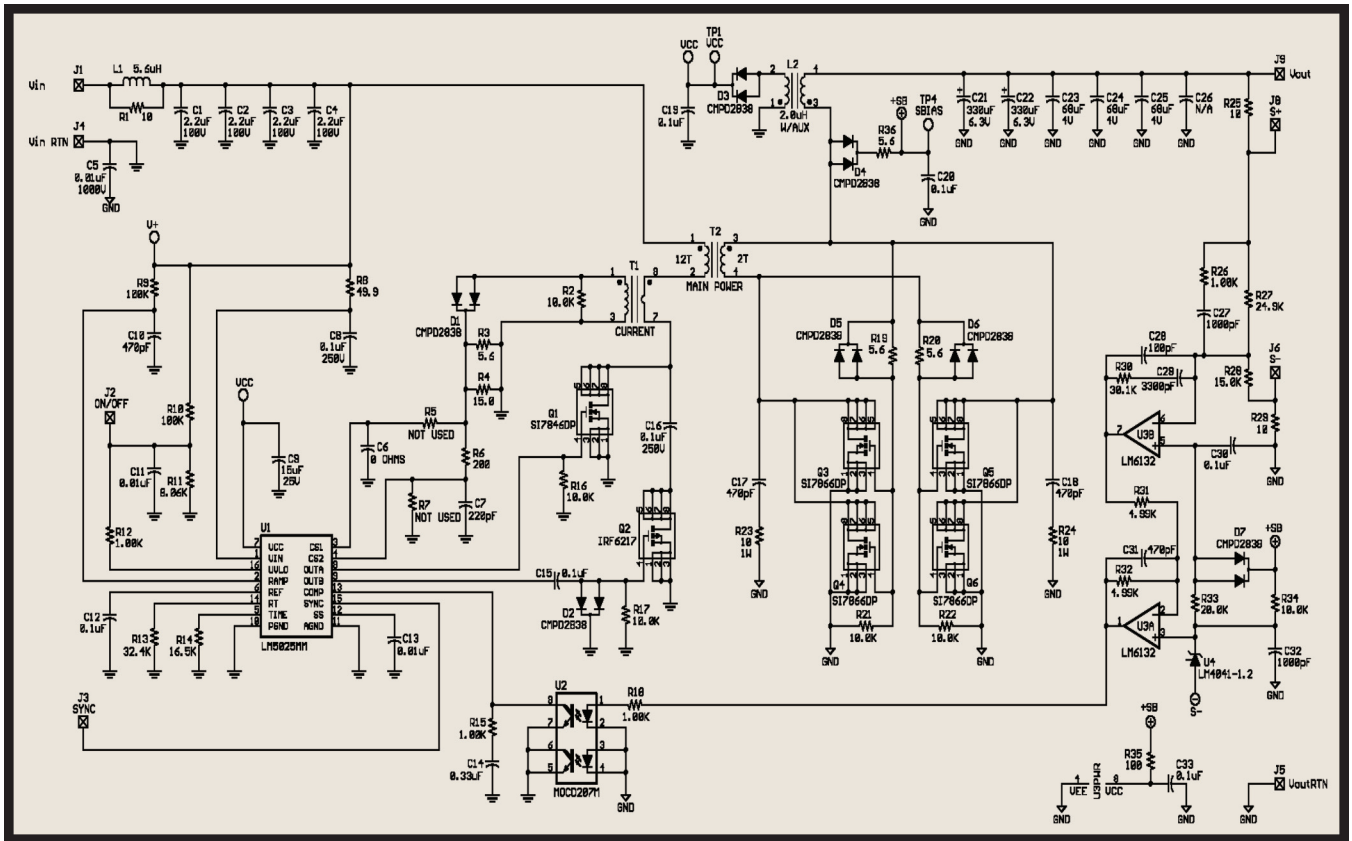


Fig. 6. Active clamp-based forward converter.

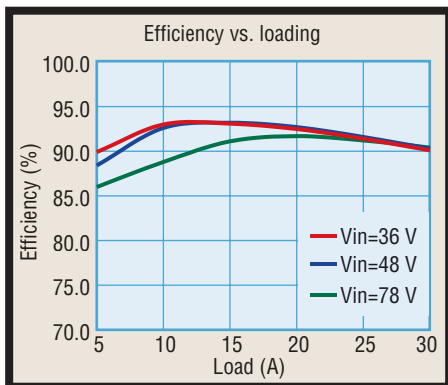


Fig. 7. Demonstration converter efficiency.

insulated copper stampings.

The LM5025 controller directly drives the n-channel power switch and a p-channel reset switch, using a compound gate driver architecture. The internal gate drivers are sized differently for each switch. The

reset switch only carries the magnetizing current, allowing smaller device size and gate drive requirements. The main switch requires a robust gate drive in order to achieve the reduction in switching losses. The necessary timing delay between each of the gate driver outputs is programmable within the controller.

Note that the output rectifiers shown in the block diagrams have been replaced by synchronous MOSFETs. For low-output voltage applications, the use of these devices significantly increases the overall efficiency. The active reset scheme eases the implementation of sync rectifiers because they can be self-driven. The sync rectifier gates are driven directly from the transformer secondary, as shown.

During the power switch on time, Q5 and Q6 are ac-

tive with a gate voltage of $V_{IN} \times N_s/N_p$. During the power switch-off time (reset time), Q3 and Q4 are active with a gate drive voltage of:

$$\frac{V_{out}}{\left(1 - \frac{V_{out}}{V_{in}} \cdot \frac{N_p}{N_s}\right)}$$

The transformer turns ratio (N_p/N_s) for this design is six. The range of gate drive voltage for the forward sync rectifiers, Q5 and Q6, is 6 V to 12.5 V. The range of gate drive voltage for the freewheeling sync rectifiers, Q3 and Q4, is 4.5 V to 7.3 V. Fig. 7 shows the measured efficiency at three different input voltages vs. load current. The peak efficiency of 93% occurs at mid-loading range.

There are several variations of this technique, such as active clamp flyback and active clamp forward using an n-channel reset switch. Although not covered in this article, these variations also provide efficiency benefits. The active clamp technique allows the use of lower-voltage-rated MOSFETs and eases the use of self-driven synchronous rectifiers. The magnetizing and leakage energies are recycled and returned to the source. These benefits extend the power-conversion efficiency.

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