

Printed Wiring Board Manufacturing Advances

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Heavy copper circuit boards dramatically increase power handling and provide a robust platform for extreme conditions.

Various new power electronics products are being designed every day for a range of applications. Increasingly, these projects are taking advantage of a new trend in the printed wiring

board (PWB) industry: heavy copper circuits.

What defines a heavy copper circuit? Most commercially available PWBs are manufactured for low-voltage/low-power applications, with copper traces/planes made up of copper weights ranging from 0.5 oz/ft² to 3 oz/ft². A heavy copper circuit is manufactured with copper weights anywhere between 4 oz/ft² to 60 oz/ft². The increased copper weight combined with a suitable substrate transforms the once unreliable, weak circuit board into a durable and reliable wiring platform.

The construction of a heavy copper circuit endows a board with benefits such as:

- Increased resistance to thermal strains.
- Increased current carrying capacity.
- Increased mechanical strength at connector sites and in PTH holes.



Fig. 1. Process coupon of a hybrid thick/thin copper printed wiring board (solder coated).

- Use of exotic materials to their full potential (i.e., high temperature) without circuit failure.
- Reduced product size by incorporating multiple copper weights on the same layer of circuitry (Fig. 1).
- Heavy copper plated vias help to transfer heat to an external heatsink.
- On-board heatsinks directly plated onto the board surface using up to 60-oz copper planes.
- On-board high-power-density planar transformers.

Although the disadvantages are few, it's important to understand the heavy copper circuit's basic construction to fully appreciate its capabilities and potential applications.

Heavy Copper Circuit Construction

Standard printed wiring boards, whether double-sided or multilayer, are manufactured using a combination of copper etching and plating processes. Circuit layers start as thin sheets of copper foil (generally 0.5 oz/ft² to 2 oz/ft²) that are etched to remove unwanted copper, and plated to add copper thickness to planes, traces, pads and plated-through holes. All of the circuit layers are laminated into a complete package using an epoxy-based substrate, such as FR4 or polyimide.

Boards incorporating heavy copper circuits are produced in exactly the same way, albeit with specialized etching and plating techniques, such as high-speed/step plating and differential etching. Historically, heavy copper features were formed entirely by etching thick copper-clad laminated board material, causing uneven trace sidewalls and unacceptable undercutting. Recent advances in plating technology have allowed heavy copper features to be formed with a combination of plating and etching, resulting in straight sidewalls and negligible undercut. Plating of a heavy copper circuit enables the board fabricator to increase the amount of copper thickness on plated holes and via sidewalls.

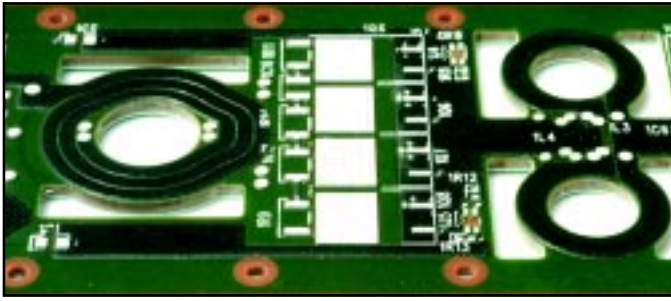


Fig. 2. Embedded planar transformers.

It's now possible to mix heavy copper with regular features on a single board. Advantages include reduced layer count, low impedance power distribution, smaller footprints and potential cost savings. Normally, high-current/high-power circuits and their control circuits were produced separately on separate boards. Heavy copper plating makes it possible to integrate high-current capacity circuits and control circuits to realize a highly dense yet simple board structure.

The heavy copper features can be seamlessly connected to regular circuits because standard PWB manufacturing rules apply. Heavy copper and regular features can be placed freely without restriction, provided the designer and fabricator discuss manufacturing tolerances and abilities prior to final design (Fig. 1).

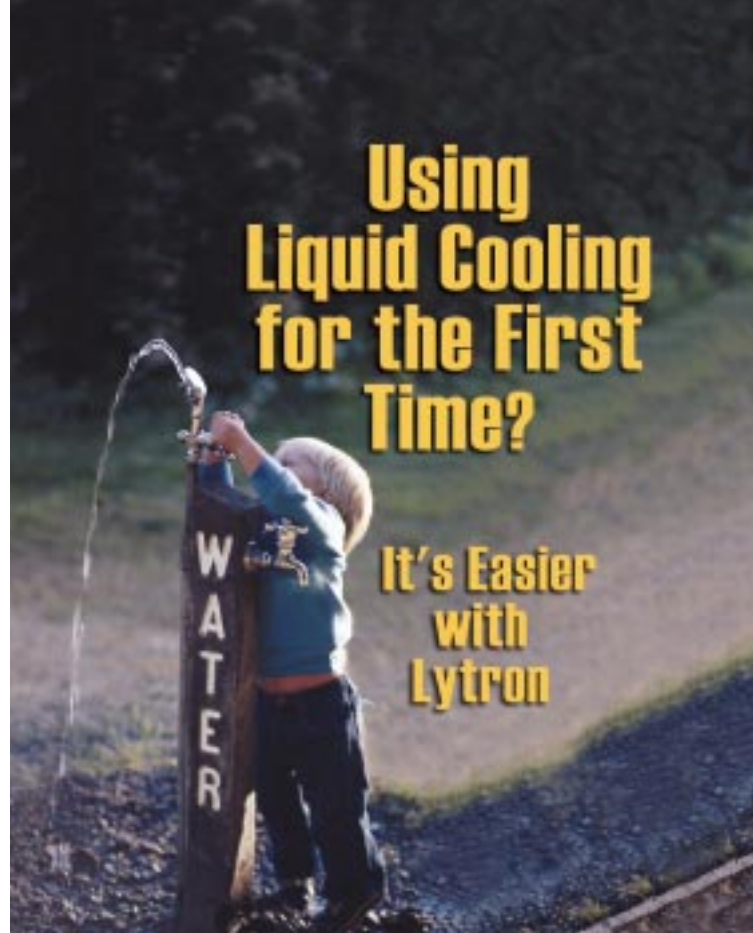
Current Carrying Capacity and Temperature Rise

What amount of current can a copper circuit safely carry? This is a question often voiced by designers who wish to incorporate heavy copper circuits into their project. This question is usually answered with another question: How much heat rise can your project withstand? This question is posed because heat rise and current flow go hand in hand. Let's try to answer both of these questions together.

When current flows along a trace, there is an i^2R (power) loss that results in localized heating. The trace cools by conduction (into neighboring materials) and convection (into the environment). Therefore, to find the maximum current a trace can safely carry, we must find a way to estimate the heat rise associated with the applied current. An ideal situation would be to reach a stable operating temperature where the rate of heating equals the rate of cooling. There has been some work done on this subject and a model has been developed.

$$I = 0.025 * \Delta T^{0.45} W^{0.79} Th^{0.53} \quad (Eq.1)^{[1]}$$

where I is current (A), ΔT is temperature rise ($^{\circ}C$), W is width of the trace (mil) and Th is thickness of the trace (mil). This model is based on extensive testing of external traces; internal traces should be derated by 50% (estimate) for the same degree of heating. The table shows the current carrying capacity of several traces of differing cross-sectional areas.



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$\Delta T(^{\circ}C)$	Trace Width (mil)	Trace Thickness (oz/ft ²)	Location (external/internal)	Max Current (Amps)
20	50	1	External	2.629
20	50	10	External	9.137
20	500	1	External	14.663
20	500	10	External	50.958
20	2000	1	External	48.121
20	2000	10	External	167.237
50	50	1	External	3.996
50	50	10	External	13.888
50	500	1	External	22.288
50	500	10	External	77.459
50	2000	1	External	73.146
50	2000	10	External	254.209

Current carrying capacity of various copper trace sizes.

What is an acceptable amount of heat rise will differ from project to project. Most circuit board dielectric materials can withstand temperatures of 100°C above ambient, although this amount of temperature change would be unacceptable in most situations. Equation 1 can be rearranged to show that ΔT is directly proportional to power (I^2R), which acts to heat the trace, and inversely proportional to the square root of W (surface area), which helps to cool the trace. The results of this analysis lead to a fairly reasonable, intuitive understanding of the dynamics involved.

We can take equation 1 a step further to find the fusing current of a copper trace. Using the melting point of copper (1083°C) and assuming ambient temperature to be 20°C, the result is:

$$I = 0.57528 * W^{0.79} Th^{0.53} \quad (\text{Eq. 2})$$

where I , W and Th are defined as in equation 1. Another useful equation developed by M. Onderdonk relates current to the time it takes for a copper wire to melt:

$$I = 0.188 * A / t^{0.5} \quad (\text{Eq. 3})$$

where A is cross-sectional area (square mils), I is current (A) and t is time (seconds).

Circuit Board Strength and Survivability

Circuit board manufacturers and designers can choose from a variety of dielectric materials, from standard FR4 (operating temp. 130°C) to high-temperature polyimide (operating temp. 250°C). A high-temperature or extreme environment situation may call for an exotic material, but if the circuit traces and plated vias are standard 1-oz/ft² copper, will they survive the extreme conditions?

The circuit board industry has developed a test method for determining the thermal integrity of a finished circuit product. Thermal strains come from various board fabri-

cation, assembly and repair processes, where the differences between the coefficient of thermal expansion (CTE) of Cu and the PWB laminate provide the driving force for crack nucleation and growth to failure of the current-carrying capability of the board. thermal cycle testing (TCT) checks for an increase in resistance of a circuit as it undergoes air-to-air thermal cycling from 25°C to 260°C.

An increase in resistance indicates a breakdown in electrical integrity via cracks in the copper circuit. A standard coupon design for this test incorporates a chain of 32 plated through holes, which has long been considered to be the weakest point in a circuit when subjected to thermal stress. TCT studies done on standard FR4 boards

with 0.8-mil to 1.2-mil copper plating have shown that 32% of circuits fail after eight cycles (a 20% increase in resistance is considered a failure).

TCT studies done on exotic materials show significant improvements to this failure rate (3% after eight cycles for Cyanate Ester), but are prohibitively expensive (five to 10 times material cost) and difficult to process. An average surface-mount technology assembly sees a minimum of four thermal cycles before shipment, and could see an additional two thermal cycles for each component repair.

It's not unreasonable for a SMOBC board that has gone through a repair and replacement cycle to reach a total of nine or 10 thermal cycles. The TCT results clearly show that the failure rate, no matter what the board material, can become unacceptable.

Printed circuit board manufacturers know that copper electroplating isn't an exact science—changes in current densities across a board and through numerous hole/via sizes result in copper thickness variations of up to 25%. Most areas of "thin copper" are on plated-hole walls—the TCT results clearly show this to be the case.

Using heavy copper circuits would reduce or eliminate these failures altogether. An additional 1 oz/ft² of plated copper to a hole wall reduces the failure rate to almost zero (TCT results show a 0.57% failure rate after eight cycles for standard FR4 with a minimum of 2.5-mil copper plating). In effect, the copper circuit becomes impervious to the mechanical stresses placed on it by the thermal cycling.

Thermal Management

As designers strive to obtain maximum value and performance from their projects, printed circuits are becoming more complex and are placed in ever-decreasing space. Miniaturization, use of power components, extreme environmental conditions and high-current requirements increase the importance of thermal management. The high power loss in the form of heat that's often

generated in the operation of electronics has to be dissipated from its source and radiated to the environment; otherwise, the components could overheat and failures may result. However, heavy copper circuits can help to dissipate heat away from valuable components, reducing failure rates dramatically.

In order to achieve proper heat dissipation from heat sources in and on the surface of a circuit board, heatsinks are employed. The purpose of any heatsink is to dissipate heat away from the source of generation by conduction and emit this heat by convection to the environment owing to a large surface area to the ambient air. The heat source on one side of the board (or internal heat sources) is connected by copper vias (sometimes called "heat vias") to a large bare copper area on the other side of the board.

Generally, classical heatsinks are bonded to this bare copper surface by means of a thermally conductive adhesive, or in some cases, are riveted or bolted. Most heatsinks are made of either copper or aluminum. The assembly process required for classical heatsinks consists of three labor-intensive and costly steps.

To begin, the metal serving as the heatsink must be punched or cut to the required shape. The adhesive layer must also be cut or stamped for a precision fit between the circuit board and the heatsink. Last but not least, the heatsink must be properly positioned on the PWB and the entire package has to be coated for electrical and/or corrosion resistance with a suitable lacquer or cover coat.

Normally, the above process can't be automated and must be done by hand. The time and work required to complete this process is significant, and the results are poorer than a mechanical, automated production.

In contrast, built-in heatsinks are created during the printed circuit board manufacturing process and require no additional assembly. Heavy copper circuit technology makes this possible. This technology allows the addition of thick copper heatsinks virtually anywhere on the outer surfaces of a board. The heatsinks are electroplated on the surface and thus connected to the heat conducting vias without any interfaces that impede thermal conductivity.

Another benefit is the added copper plating in the heat vias, which increases heat conduction to the board design, realizing that they can expect the same degree of accuracy and repeatability inherent in PWB manufacturing. Because planar windings are actually flat conductive traces formed on copper clad laminate, they improve the overall current density compared to cylindrical wire conductors. This benefit is due to minimization of skin effect and higher current-carrying efficiency.

On-board planars achieve excellent primary-to-secondary and secondary-to-secondary dielectric isolation because the same dielectric material is used between all layers, ensuring complete encapsulation of all windings. In addition, primary windings can be spilt so that the secondary windings are sandwiched between the primaries,

achieving low leakage inductance. Standard PWB lamination techniques, using a choice of a variety of epoxy resins, can safely sandwich up to 40 layers of copper windings as thick as 7 oz/ft².

During the manufacture of heavy copper circuits, we are usually dealing with significant plating thicknesses; therefore, allowances must be made in defining trace separations and pad sizes. For this reason, designers are advised to have the board fabricator on board early in the design process. UPE Inc. has developed a set of design guidelines for heavy copper circuits that give designers a basic overview of what is required.

Power electronics products using heavy copper circuitry have been in use for many years in the aeronautical industry and are gaining momentum as a technology of choice in military applications. It's believed that market requirements will extend the application of this type of product in the near future.

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