Overpower Compensation for Current-Mode Supplies

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A current-mode power supply works by observing the peak current circulating in an inductance. By adjusting the peak current setpoint at which the power switch turns off, the feedback loop is able to regulate the power flow to a given load. However, situations exist where the loop asks for the maximum output power. This can occur during startup, or when the converter experiences an overload or short circuit. Unfortunately, the internal circuitry inside a pulse width modulation (PWM) controller includes several cascaded logic gates that hamper the controller's reaction time.

Fig.1 shows a simplified arrangement for the NCP1200 fixed-frequency controller from ON Semiconductor. When the voltage developed across R_{sense} reaches the setpoint imposed on the inverting input of ICOMP, its output goes high and resets the latch. Then, Q goes low, as does the driver's output. The time required for this series of events within the controller is called the propagation delay (t_p). Put another way, t_p describes how long it takes to bring the MOSFET gate low when an overcurrent condition is sensed on the CS pin.

Typically, this propagation delay t_p is around 160 ns max over a fixed 1-nF load. Therefore, when the current ramps up, the controller will take time before stopping the pulses. During this time, the current will continue rising, as depicted in Fig. 2. In a real application, the driver loading isn't a fixed but a nonlinear capacitance whose charge in the enhancement mode is expressed by the Q_g parameter.

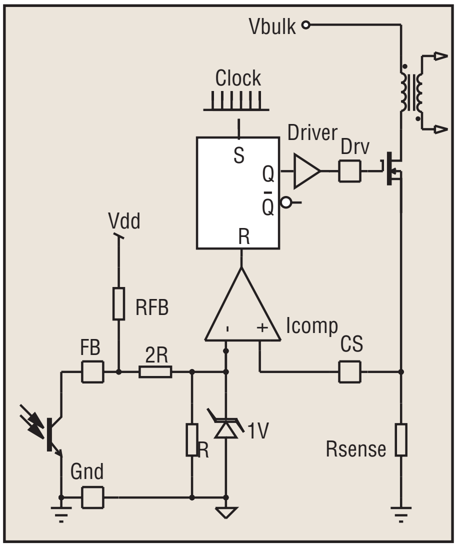

Fig. 1. *A current-mode PWM converter includes a latch and a fast comparator.*

For example, a Q_g of 50 nC for a 10-V V_{GS} is the equivalent of a Q / V = 5-nF capacitor. If the designer now inserts a 22-Ω resistor in series with the gate to calm down spurious oscillations, then we end up with the addition of another delay. In the case of a 22-Ω resistor and a 5-nF capacitor, the total delay t_{ptot} becomes $t_p + t_{RgateCgate}$ or 160 ns + 100 ns = 260 ns.

In normal operation, when the power supply regulates, this drawback is permanently compensated by the loop, which slightly lowers the feedback voltage since I_{p2} matters (Fig. 2). In short-circuit or in overload conditions, the feedback loop has been lost and the peak current should be limited by the 1-V clamp: $I_p(max) = 1 / R_{sense}$. The propagation delay will alter this value, depending on the current slope.

The on-time inductor slope S_L in a converter is a function of the voltage applied across the inductor and the inductor value itself when the power switch is closed. In a flyback converter, the slope is V_{bulk} / L (Eq. 1), while in a buck converter it would be $(V_{in}-V_{out})$ / L and so on in the various converter configurations. In the Fig. 2 example, I_{p2} would be related to I_{p1} via:

$$I_{p2} = I_{p1} + S_L \times t_{ptot}. \quad \text{(Eq. 2)}$$

To see the effect of the propagation delay, let's take the example of a flyback converter designed to operate from a universal input of 85 Vac to 265 Vac with the following operating conditions:

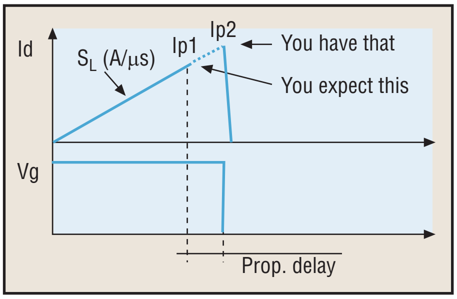

Fig. 2. *Effect of propagation delays.*

- Low line rectified voltage (Vin DC_{LL}) = 120 V
- High line rectified voltage (Vin DC_{HL}) = 374 V
- Efficiency (η) = 85% at low line and 87% at high line
- Primary inductance (L_p) = 180 µH
- Primary sense resistor (R_{sense}) = 0.33 Ω
- Switching frequency (F_{sw}) = 60 kHz
- Controller propagation delay, worse case (t_p) = 160ns
- Gate resistor = 22 Ω
- MOSFET gate charge (Q_g) = 100 nC
- Total propagation delay including $R_{gate}C_{Qg}$ network t_{ptot} = 160 + 200 = 360 ns
- Maximum set point = 1 V.

In a flyback converter operating in discontinuous conduction mode (DCM), transmitted output power is calculated as:

$$P_{out} = \eta \times 0.5 \times L_p \times I_{p^2} \times F_{sw} \quad \text{(Eq. 3)}$$

In overload, just before the controller internal protection trips, the maximum current set point imposes a 1-V level over R_{sense}. In our example, it implies a 1/0.33 = 3-A peak current. However, we need to account for the total propagation delay that alters this number at both line levels:

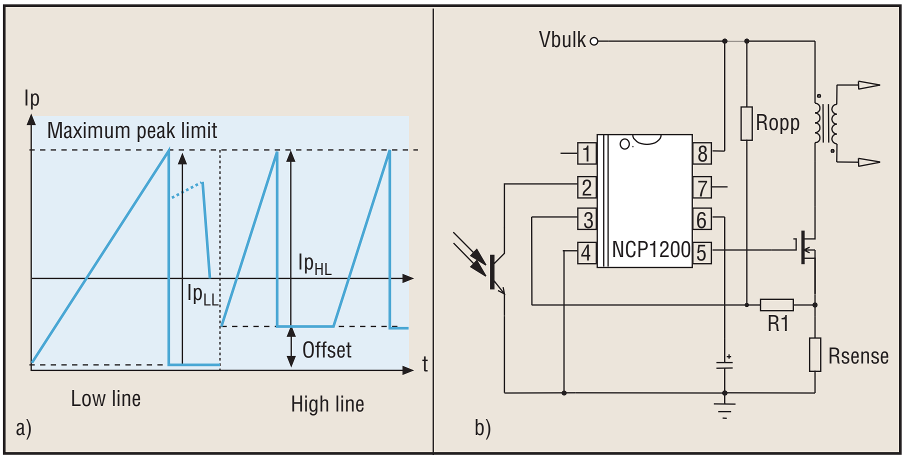

Fig. 3. *Overpower protection (OPP) adds an offset proportional to the input line to reduce the available peak current at high line (a). OPP also can be implemented using the NCP1200 (b).*

$$3 + 360\text{ ns} \times 120\text{ V}/ 180\text{ µH} = 3.24\text{ A at } 120\text{ Vdc} \quad \text{(Eq. 4)}$$

and

$$3 + 360\text{ ns} \times 374\text{ V} / 180\text{ µH} = 3.75\text{ A at } 374\text{ Vdc} \quad \text{(Eq. 5).}$$

We can therefore calculate the delivered power at low line and high line, assuming the power supply stays in DCM at low line:

$$P_{low\ line} = 0.5 \times 0.85 \times 3.24^2 \times 180\ \mu \times 65\text{ k} = 52.2\text{ W} \quad \text{(Eq. 6)}$$

$$P_{high\ line} = 0.5 \times 0.87 \times 3.75^2 \times 180\ \mu \times 65\text{ k} = 71.6\text{ W} \quad \text{(Eq. 7)}$$

There is an almost 20-W power difference between the two levels or a 37% increase in power capability at high line. In some applications, where the output current must absolutely stay below a safe value, this isn't acceptable.

To circumvent this problem, we could think of reducing the current clamp from its maximum value at low line (1 V in our example) down to another value, such as 0.85 V at high line. However, we don't have access to this clamp, so to achieve this effect we would need to sense the bulk voltage via a dedicated pin on the controller.

A more practical alternative is overpower protection, OPP. It consists of offsetting the voltage sense from its floor point, since we cannot touch the ceiling point. Fig. 3a illustrates how it works. This method requires that equation 7 equal what the power supply delivers at low line:

$$0.5 \times 0.87 \times Ip_{HL}^2 \times 180\text{ u} \times 65\text{ k} = 52.2\text{ W}$$

$$\rightarrow Ip_{HL} = (52.2/(0.5 \times 0.87 \times 65\text{ k} \times 180\text{ u})) = 3.2\text{ A}$$

where the slight difference from the previous result is due to the efficiency variation between high and low line. From equation 5, Ip_{HL} corresponds to a controller imposed peak current of 3.2 – 360 n × 374/180 µ = 2.45 A.

Because the controller deals with voltages, 2.45 A over a 0.33-Ω resistor means 808 mV. From the maximum 1-V set point, we need to create an offset of 1 – 808 mV = 191.5 mV at V_{bulk} = 374 Vdc. If we fix R1 to 1 kΩ, then R_{OPP} can be found to be:

$$(374-0.1915) / (0.1915 / (0.33 + 1k)) = 1.95\text{ M}\Omega.$$

At low line, the remaining offset will be:

$$120 \times (1000.33 / (1000.33 + 1.95\text{ M})) = 61.5\text{ mV}.$$

The peak current at low line now becomes:

$$(1 - 61.5\text{ m}) / 0.33 + 120 \times 360\text{ n}/ 180\ \mu = 3.083\text{ A}.$$

Compared to 3.24 A before compensation, it corresponds to a final power decrease of 10% (P_{out} = 47.3 W). Original specs need to be checked to see if it still meets them. If not, R_{OPP} will be slightly increased.

A mean exists to compensate the propagation delay influence in a current-mode converter. Here, the DCM mode was covered but the analysis still holds in continuous conduction mode (CCM), where the power transfer becomes:

$$Pout = \eta \times 0.5 \times L_p \times (I_{p1}^2 - I_{p2}^2) \times Fs_w$$

and where I_{p1} and I_{p2}, respectively, represent the peak and valley currents in the primary inductor. For a lower standby power, V_{bulk} can be replaced by its image obtained from an auxiliary winding wired in forward mode. In that case, the rectified auxiliary will be N × V_{bulk}. The power consumed by R_{OPP} will greatly be reduced. **PETech**

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