

# Capacitor Ripple Current Improvements

By **Jim Drew**, Hardware Engineer VII, Hewlett-Packard, Marlboro, Mass.

The multiphase buck regulator topology allows a reduction in the size of the input and output capacitors versus single-phase designs. By quantifying the input and output currents, designers can determine the requirements for the input and output capacitors.

**I**n the conventional dc-dc converter buck topology (Fig. 1), power from the input voltage source is transferred to the output filter by turning on the pass transistor. When the pass transistor is on, the voltage across the output inductor is the difference between the input voltage and the output voltage, causing the inductor current to ramp up and store more energy in the inductor. While the current through the inductor is below  $I_{o,avg}$ , the capacitor is supplying the additional load current. When the inductor current is greater than  $I_{o,avg}$ , the additional current through the inductor recharges the output capacitor.

After a predetermined time,  $T_{on} = T_p \cdot (V_o/V_{in})$ , where  $T_p$  is the period of the switching frequency, the pass transistor is turned off and the shunt transistor is turned on. The voltage across the inductor is now minus  $V_o$ , resulting in a downward slope in the inductor current. The inductor is now transferring its stored energy to the load and continues to charge the output capacitor, until the inductor current becomes less than  $I_{o,avg}$ .

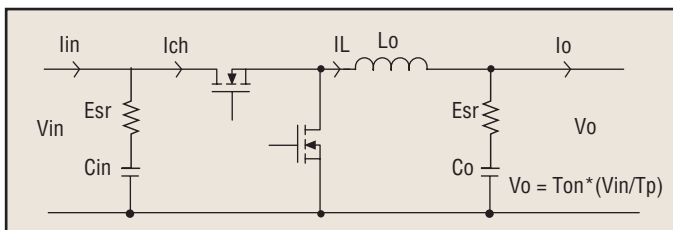


Fig. 1. Conventional buck converter topology.

The shunt transistor remains on during the time period of  $T_{off} = T_p - T_{on}$ . As a result, the input current through the pass transistor of the conventional dc-dc converter buck topology (Fig. 1) is a clipped trapezoidal waveform (Fig. 2), which is the composite of the load current

and the inductive ramp current of the magnetic elements in the load current path.

The period of this current waveform is the output switching period of the pass transistor. The duty cycle is related to the ratio of the output voltage to the input voltage. Because the switching frequency of the dc-dc converter is beyond the response time of the input source and the power distribution system, this current must be supplied by the input capacitor of the dc-dc converter. The RMS current drawn from the input capacitor and (to a lesser degree) the ripple voltage across the input capacitor are key factors determining the selection of this capacitor.

The output capacitor usually is determined from the output ripple voltage specification, whose major influencing factor is the output inductor ripple current (Fig. 3) flowing through the effective series resistance of the output capacitor. In low-output voltage applications, the required output ripple voltage is only met by increasing the size of the output inductor, lowering the output ripple current or paralleling many output capacitors.

The output impedance of the converter is the square

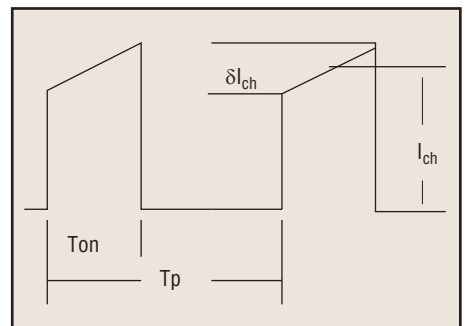


Fig. 2. Input pulse current.

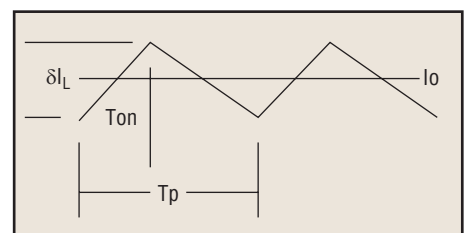


Fig. 3. Output inductor ripple current.

root of the ratio of the output inductance and the output capacitance. Increasing the size of the output inductor is generally a poor choice because of its effect on the output impedance, transient response and its physical size. Paralleling of output capacitors results in reducing output ripple voltage and output impedance.

## Multiphase Topology

Fig. 4 shows the basic circuit of each channel, while Fig. 5 shows a 4-channel system. Each channel's switching cycle is delayed in time by the channel switching period divided by the number of channels. Evaluating the ratio of the input voltage to the output voltage to the nearest integer is one method to define the number of channels, resulting in the lowest output ripple current.

In the multiphase topology, the load current is the sum of the average channel currents. Evaluating the ratio of the total output current to the channel current to the nearest integer is another method to define the number of channels, which may result in a higher output

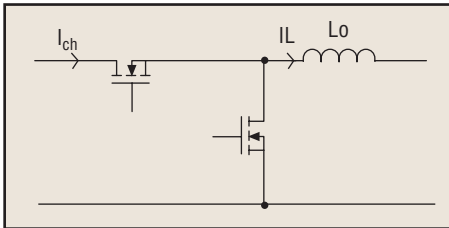


Fig. 4. Basic channel circuit.

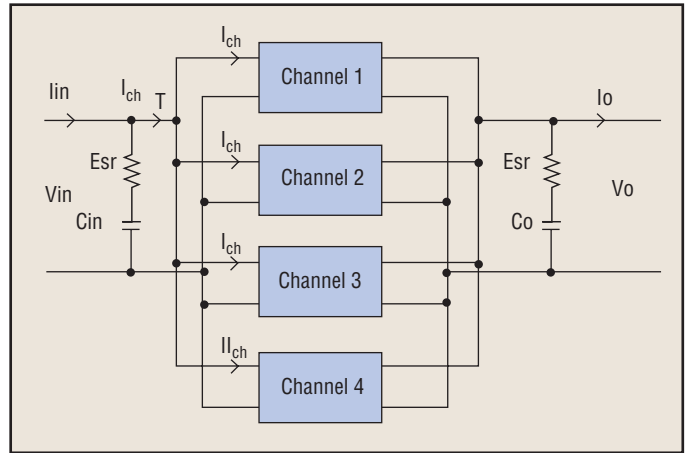


Fig. 5. Four-channel multiphase buck regulator.

ripple current. For a multiphase converter with four channels with each channel switching at 250 kHz, the switching period would be 4  $\mu$ s and each channel would be time-delayed by 1  $\mu$ s. This would result in an output and input current ripple frequency of 1 MHz.

The effect of time delaying is that the input current waveform changes from a clipped trapezoid to a sawtooth shifted by a dc component (Fig. 6), when the product of the number of channels and the channel duty cycle is an integer. When the product is less than one, it remains

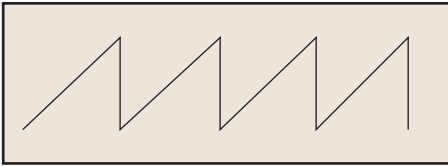


Fig. 6. Input current for  $N \cdot D = \text{integer}$ .

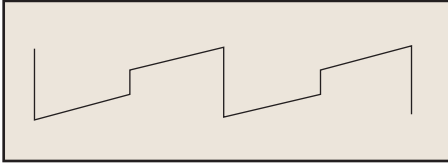


Fig. 7. Input current  $N \cdot D > 1$  but not an integer.

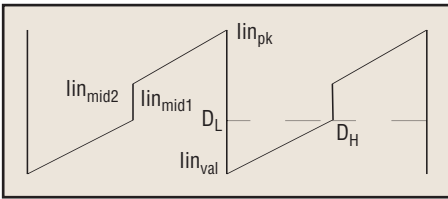


Fig. 8. Input current for  $N \cdot D > 1$  but not an integer.

a clipped trapezoid but at a frequency of four times the channel frequency. In all other cases where the product is greater than one but not an integer, the waveform is a modified sawtooth plus a dc component (Fig. 7). The output current triangular wave amplitude also is reduced. In fact, the output current triangular wave amplitude is reduced to zero

dominant power losses, we can calculate the maximum allowable  $R_{ds(on)}$  and the on time ( $T_{on_{ch}}$ ) of the buck FET. We'll select a FET with an  $R_{ds(on)}$  of 5 mΩ.

$$R_{dson} = \frac{V_o \cdot (1 - Eff)}{I_o}$$

$$T_{on_{ch}} = \frac{V_o + R_{dson} \cdot I_o}{V_{in} \cdot f_{ch}}$$

Based on the output ripple voltage requirements, we can select the number of required capacitors with the following expression. The required number of capacitors will be rounded up to the next integer—in this case, 17.

$$N_{Co} = \frac{Esr \cdot \Delta I_{ch} + \frac{1}{C} \cdot \int_0^{T_{on_{ch}}} \frac{\Delta I_{ch} \cdot t}{T_{on_{ch}}} dt + EsL \cdot \frac{\Delta I_{ch}}{T_{on_{ch}}}}{\Delta V_o}$$

The number of input capacitors will be selected based on the capacitor ripple current requirements. The peak current ( $I_{pk_{ch}}$ ) in the channel is 14 A, while the average input current is 19 A. The input RMS ( $I_{in_{RMS}}$ ) and the capacitor RMS ( $I_{c_{RMS}}$ ) currents can now be calculated. The capacitor RMS current is 24.311 A, which sets the number of input capacitors to 14.

$$I_{in_{RMS}} = \sqrt{D_{ch} \cdot \frac{3 \cdot (I_{pk_{ch}})^2 - 3 \cdot I_{pk_{ch}} \cdot \Delta I_{ch} + \Delta I_{ch}^2}{3}}$$

dc component, when the product of the number of channels and the channel duty cycle is an integer.

The design equations used to determine the input and output currents, as well as for the selection of the input and output capacitors, can be found below. The scalars  $n_1$  (the integer of the number of phases times the duty cycle of the channel plus one) and  $n_2$  (the number of phases minus  $n_1$ ) are used to define the number of rising and falling slopes respectively from the channel output current seen in the system's output ripple current for various duty cycle ranges.

The scalar  $n_3$  ( $n_1 - 1$ ) is used to define the two duty cycles (DL and DH) of the modified sawtooth waveform of Fig. 8. The scalars  $n_3$  and  $n_4$  ( $n_3 - 1$ , if negative use 0) are used to calculate the peak and the lower midpoint of the input current, by determining the number of rising slopes from the channel input current seen in the system's input current for various duty cycle ranges.  $T_{on_{out}}$  is the time duration of the rising slope of the output ripple current.

### Design Example

The results of a design example will be presented for a nonisolated buck converter whose input is a 5-V source and whose output is 1.65 V at 50 A. It will be assumed that the conversion efficiency will be 80% and the channel operating frequency ( $f_{ch}$ ) will be 250 kHz. The first case will use the conventional, single-channel, buck converter, and that design will be compared to a 5-channel multiphase converter. We'll use the same inductance in both designs; therefore, the current ramp ( $\Delta I_{ch} = 8$  A) will be the same. The input and output capacitors will consist of a 470 μF 10-V capacitor that has an ESR of 60 mΩ, an ESL of 1 nH and and RMS current rating of 1.826 A at 85°C.

If we assume the conduction losses in the FETs are the

	I <sub>out</sub>	ΔI <sub>out</sub>	I <sub>Co</sub> <sub>RMS</sub>	C <sub>o</sub>	I <sub>in</sub> <sub>avg</sub>	I <sub>in</sub> <sub>RMS</sub>	I <sub>Cin</sub> <sub>RMS</sub>	C <sub>in</sub>
Conventional Topology	50 A	8 A	2.308 A	17×470 uF	19.0 A	30.855 A	24.311 A	14×470 uF
Multiphase Topology	50 A	0.611 A	0.176 A	2×470 uF	19.0 A	19.347 A	3.648 A	2×470 uF
Multiphase Simulation	50 A	0.611 A	0.176 A		19.009 A	19.365 A	3.642 A	

Table. Comparison of conventional buck topology to the multiphase buck topology.

$$I_{C_{RMS}} = \sqrt{I_{in_{RMS}}^2 - I_{in_{avg}}^2}$$

The 5-channel multiphase buck converter will have one-fifth the channel current of the conventional buck converter, resulting in an R<sub>ds(on)</sub> of 25 mΩ to meet the same efficiency requirement above. The on time of the buck FET will be the same, but the positive slope time of the current into the output capacitors will be based on the expressions below, along with its change in current.

$$T_{on_{out}} = \frac{N \cdot D_{ch} - n_3}{N \cdot f_{ch}}$$

$$\Delta I_{out} = \left[ \left( \frac{n_1 \cdot \Delta I_{ch}}{T_{on_{ch}}} - \frac{n_2 \cdot \Delta I_{ch}}{T_{off_{ch}}} \right) T_{on_{out}} \right]$$

Substituting T<sub>on<sub>out</sub></sub> for T<sub>on<sub>ch</sub></sub> and ΔI<sub>out</sub> for ΔI<sub>ch</sub> in the expression for the number of output capacitors results in two capacitors being required.

The input current will be the summation of the five, time-shifted, channel currents. The base frequency of the

input current will be the number of channels times the channel frequency while its shape is a modified sawtooth waveform. Expressions for the duty cycle of the lower rise in current (DL) and the upper rise in current (DH) are presented. These two duty cycles and the two scalars (n<sub>3</sub> and n<sub>4</sub>) are used to calculate the transition points of the input current waveform, as described in the following equations:

$$D_H = N \cdot D_{ch} - n_3$$

$$D_L = 1 - D_H$$

$$I_{in_{pk}} = I_{pk_{ch}} + \left[ \left[ (I_{pk_{ch}} - \Delta I_{ch}) + \frac{D_H}{N \cdot D_{ch}} \cdot \Delta I_{ch} \right] \cdot n_3 + \left( \sum_{A=0}^{n_4} A \right) \cdot \frac{\Delta I_{ch}}{N \cdot D_{ch}} \right]$$

$$I_{in_{val}} = I_{in_{pk}} - I_{pk_{ch}}$$

$$I_{in_{mid1}} = I_{in_{val}} + \frac{n_3 \cdot D_L}{N \cdot D_{ch}} \cdot \Delta I_{ch}$$

$$I_{in_{mid2}} = I_{in_{mid1}} + (I_{pk_{ch}} - \Delta I_{ch})$$

The input average current will be the same as the conventional buck. However, in this case, it's the product of the number of phases, the channel duty cycle and the average channel current. The expression for the input RMS current is the square root of the sum of the squares of the two trapezoidal currents that make up the input current waveform:

$$I_{in\_RMS} = \sqrt{\frac{1}{3} \cdot [(I_{in\_mid1}^2 + I_{in\_mid1} \cdot I_{in\_val} + I_{in\_val}^2) \cdot D_L + (I_{in\_pk}^2 + I_{in\_pk} \cdot I_{in\_mid2} + I_{in\_mid2}^2) \cdot D_H]}$$

The capacitor RMS current then can be found using the expression for  $I_{c\_RMS}$  above. The result of these equations was that the capacitor RMS current is 1.998 A, requiring two capacitors.

From the design example, it has been shown that the multiphase buck converter topology has reduced the required number of input capacitors from 14 to 2 and the output capacitors from 17 to 2. This has been accomplished by the reduction in ripple current seen by the input and output capacitors when the multiphase buck converter topology is employed (see the table.)

Two PSPICE models were developed to simulate the input current and the output current of the 5-channel multiphase converter to verify the calculated results. The results of the simulation agreed with the calculated results within less than a 1% error.

The increase in the output ripple frequency by the number of channels also will reduce the number of filtering capacitors at the load. Furthermore, the higher frequency will improve the response time to a load change. The control loop is allowed to have a greater bandwidth due to the higher output ripple frequency, resulting in faster transient response.

The multiphase buck converter topology also has more packaging advantages than just the reduction in the number of input and output capacitors. Each channel is converting power at a fraction of the conventional buck converter, which will reduce the size of the inductors and power MOSFETs used in the design. SMT inductors can be used along with SMT power MOSFETs (SOIC-8 package), resulting in a low-profile design. A multiphase buck converter designed to stepdown a 5-V input to 1.65-V output at 50 A has demonstrated a power-transfer efficiency of more than 80%, eliminating the need for heatsinks.

PETech

For more information on this article,  
CIRCLE 332 on Reader Service Card

**POWER  
ELECTRONICS**  
TECHNOLOGY  
EXHIBITION & CONFERENCE

November 16-18, 2004  
Navy Pier, Chicago, Illinois