

# Impedance Reflections for Multi-Output Converters

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For power supplies in which a single feedback loop governs the regulation on multiple voltage outputs, SPICE simulation can simplify and speed the stability analysis, while accounting for all possible input/output combinations.

In numerous equipment, a switch-mode power supply (SMPS) delivers various output voltages, each powering different sections. With the introduction of low-voltage circuits such as DSPs, it's not uncommon to find 1.2-V or 1.8-V supplies in addition to the standard 5-V or 12-V rails (for example, in set-top boxes or DVD players).

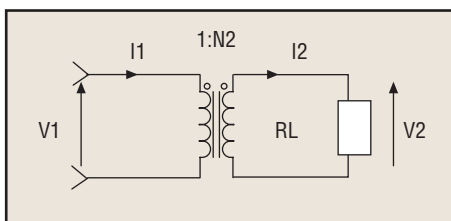


Fig. 1. Evaluating the equivalent resistance seen from the primary.

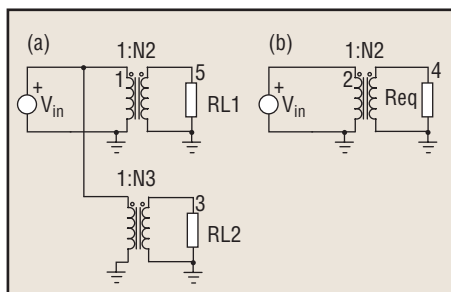


Fig. 2. When connected to an auxiliary winding,  $RL_2$  can be reflected over  $RL_1$ .

traditional paper analysis covering all possible input/output combinations is a difficult and long exercise, where simplifications can also lead to errors. Fortunately, a SPICE simulator can help shorten the stability analysis of a multi-output power supply.

In most of the cases, the regulation is performed via a feedback loop observing the voltage on a particular point, whereas the rest of the outputs trust the good performance of the transformer to keep on their respective tracks.

In this situation, the stability analysis must encompass the totality of the secondary elements to cover all possible load configurations. Naturally, a

## Simple Reflections

When a resistor is connected to a transformer secondary side, an equivalent resistor is "seen" from the primary side. Fig. 1 shows this typical example, where the turn ratio is normalized to the primary. Normalized means you divide all ratios by the primary ratio. For example,  $N_p:N_s = 10:5$ , once normalized, becomes 1:0.5.

If the transformer is perfect ( $Imag=0$ ), then we can write, assuming  $N_1 = 1$ :

$$1 \times I_1 = N_2 \times I_2 \quad (1)$$

$$\text{but also, } V_2 = V_1 \times N_2 \quad (2)$$

$$\text{or } V_1/V_2 = 1/N_2 \quad (3)$$

$$\text{Because } I_2 = V_2/RL \quad (4)$$

we can plug Equation 4 into Equation 1 to obtain:

$$I_1 = V_1/Req = N_2 \times V_2/RL \quad (5)$$

Rearranging leads to:

$$Req = V_1 \times RL/N_2 \times V_2 \quad (6)$$

Thanks to Equation 3, we finally obtain:

$$Req = RL/N_2^2 \quad (7)$$

The situation can arise when a load is connected to a secondary winding. In that case, the transformer reduction to a single winding simplifies the analysis. Fig. 2 shows a typical example.

We can first reflect  $RL_2$  on the primary side, applying Equation 7:

$$Req_1 = RL_2/N_3^2 \quad (8)$$

Then, we can "push"  $Req_1$  over  $RL_1$  by still applying Equation 7 but reversed:  $Req_2 = Req_1 \times N_2^2 = RL_2 \times N_2^2/N_3^2$ . Finally, we can write the definition of  $Req$ , as defined by Fig. 2b:

$$Req = RL_1/[RL_2 \times (N_2/N_3)^2] \quad (9)$$

In place of a resistor, we can reflect a simple capacitor (Fig. 3). In that case, for a sinusoidal excitation, where the capacitive impedance is

$$Z_c = 1/j \times C \times \omega \quad (10)$$

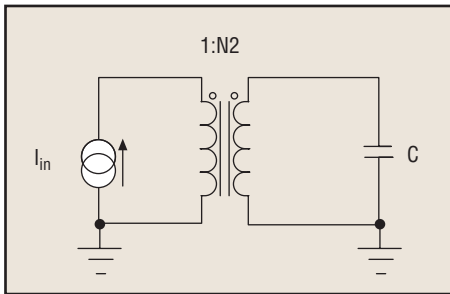


Fig. 3. A capacitor is now connected to the secondary side.

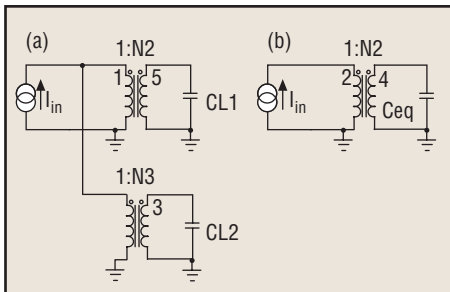


Fig. 4. When connected to an auxiliary winding, CL2 can be reflected over CL1 (a), which can be reduced to an equivalent circuit (b).

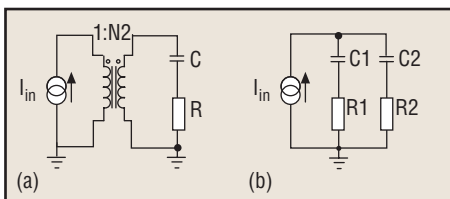


Fig. 5. A capacitor naturally exhibits an equivalent series resistance (R) (a). Paralleling two impedances does not lead to paralleling resistors and adding capacitors (b).

we can still apply Equation 7:

$$C_{eq} = 1/j \times C \times \omega \times N2^2$$

$$\text{or } C_{eq} = C \times N2^2 \quad (11)$$

On Fig. 4a, we also reflect an impedance but to another winding. Applying Equations 10 and 7, we

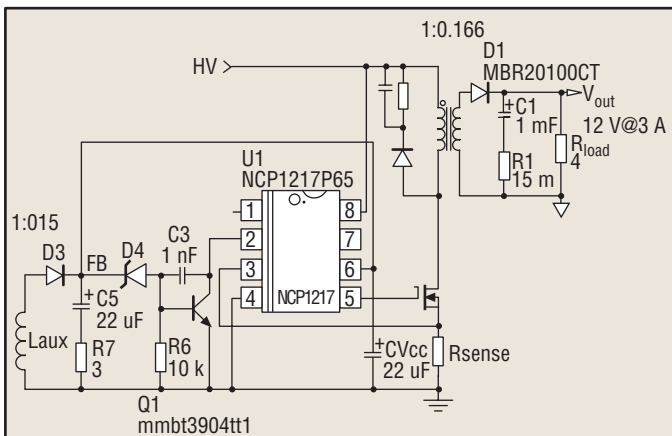


Fig. 6a. SMPS regulating from an auxiliary winding.

can show that:

$$C_{eq} = (1/j \times C \times \omega) \times [N2/N3]^2 \text{ or } C_{eq} = C \times [N3/N2]^2 \quad (12a)$$

Note that this equation is the reverse of Equation 9.

With regard to impedances, based on the above, we can write that the reflection of a given impedance to the primary side is governed by:

$$Z_{eq} = Z_{load} \times (N1/N2)^2 \quad (12b)$$

If we assume that  $N1 = 1$ , then:

$$Z_{eq} = R_{load} \times (1/N2)^2 \text{ for a resistor} \quad (12c)$$

$$Z_{eq} = 1/(2 \times \pi \times f \times C_{load} \times N2^2) \text{ for a capacitor} \quad (12d)$$

$$Z_{eq} = 2 \times \pi \times f \times L_{load}/N2^2 \text{ for an inductance} \quad (12e)$$

Because a capacitor is always associated with an equivalent series resistance (ESR), we can update Fig. 3, as Fig. 5a depicts.

The association in series of a capacitor C and a resistor R leads to a complex admittance Y defined by:

$$Y = \frac{C \cdot p}{1 + R \cdot C \cdot p} \text{ or } \frac{C \cdot p}{1 + \tau \cdot p} \quad (13)$$

if  $\tau = R \times C$ , the network time constant. Its impedance Z is then:

$$Z = \sqrt{R^2 + \left(\frac{1}{C \times \omega}\right)^2} \quad (14)$$

If we apply Equation 7, we find that the equivalent impedance seen from the primary is:

$$Z_{eq} = \sqrt{\left(\frac{R}{N2^2}\right)^2 + \left(\frac{1}{C \times \omega \times N2^2}\right)^2} \quad (15)$$

As Fig. 5b shows, paralleling complex impedances is also common because this happens when paralleling two capacitors af-

ected by individual ESRs. Unfortunately, the total impedance obtained via this element combination isn't a simple expression. Let us derive admittance expressions, easier to manipulate when impedances are in parallel.

In the first case, we assume  $R1 \times C1 = R2 \times C2$ . From Fig. 5b, Y1 is the admittance of R1.C1 and Y2 of R2.C2. Therefore,  $Y_{tot} = Y1 + Y2$ .

$$Y_{tot} = \frac{1}{R1 + \frac{1}{C1 \cdot p}} + \frac{1}{R2 + \frac{1}{C2 \cdot p}}$$

$$= \frac{1}{\frac{R1 \cdot C1 \cdot p + 1}{C1 \cdot p}} + \frac{1}{\frac{R2 \cdot C2 \cdot p + 1}{C2 \cdot p}} \quad (16)$$

$$= \frac{C1 \cdot p}{R1 \cdot C1 \cdot p + 1} + \frac{C2 \cdot p}{R2 \cdot C2 \cdot p + 1}$$

By using Equation 13 notation, we can rewrite Equation 16 via:

$$Y_{tot} = \frac{C1 \cdot p}{\tau1 \cdot p + 1} + \frac{C2 \cdot p}{\tau2 \cdot p + 1}$$

If  $\tau1 = \tau2 = \tau$ , then, the final admittance simplifies to:

$$Y_{tot} = \frac{(C1 + C2) \cdot p}{1 + \tau \cdot p} \quad (17)$$

which looks like Equation 13 where the capacitor C is the sum of both capacitors (as if paralleled) and the ESR is the value that once combined with  $(C1 + C2)$  gives  $\tau1$  or  $\tau2$ . This resistance is simply  $Req = \tau1/(C1 + C2)$ , which also leads to  $Req = R1/R2$  (which makes sense because, as F approaches infinity, both capacitors become shorts).

When two series RC networks  $R1 - C1$  and  $R2 - C2$  of same time constants are paralleled, the resulting equivalent series RC network is made

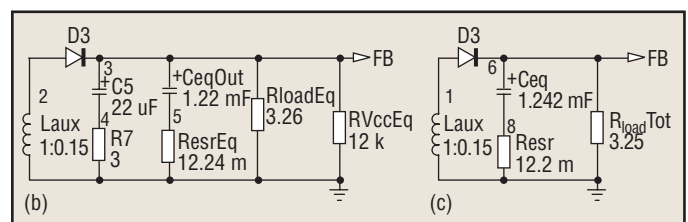


Fig. 6b. Creating a circuit equivalent to that of Fig. 6a. First step consists of reflecting all elements to the auxiliary side (b). Second step combines all elements, applying the simplification described in the text (c).

of  $C = C1 + C2$  and  $R = R1/R2$ .

In the second case, we assume  $R1 \times C1 \neq R2 \times C2$ . Starting from Equation 16, we can combine after simplification by "p" and neglecting the "1" in the expression:

$$Y_{tot} = \frac{(C1+C2)+p \cdot (\tau1 \cdot C2 + \tau2 \cdot C1)}{\left( \frac{\tau1 \cdot \tau2}{(\tau1+\tau2)} \cdot p+1 \right) \cdot (\tau1+\tau2)} \quad (18)$$

which differs from Equation 13.

In conclusion, two paralleled RC networks of different time constants do not reduce to a single RC network.

### Simplifying Analysis

A classical situation is the primary regulated power supply. In this application, the auxiliary winding not only provides the Vcc self-supply of the controller, but also offers an image of the output voltage. If the coupling between the two considered windings is of good quality, levels can track each other fairly well.

Fig. 6a depicts a flyback power supply built with the NCP1217 controller from ON Semiconductor. The feedback is ensured by a Zener diode, associated with a low-

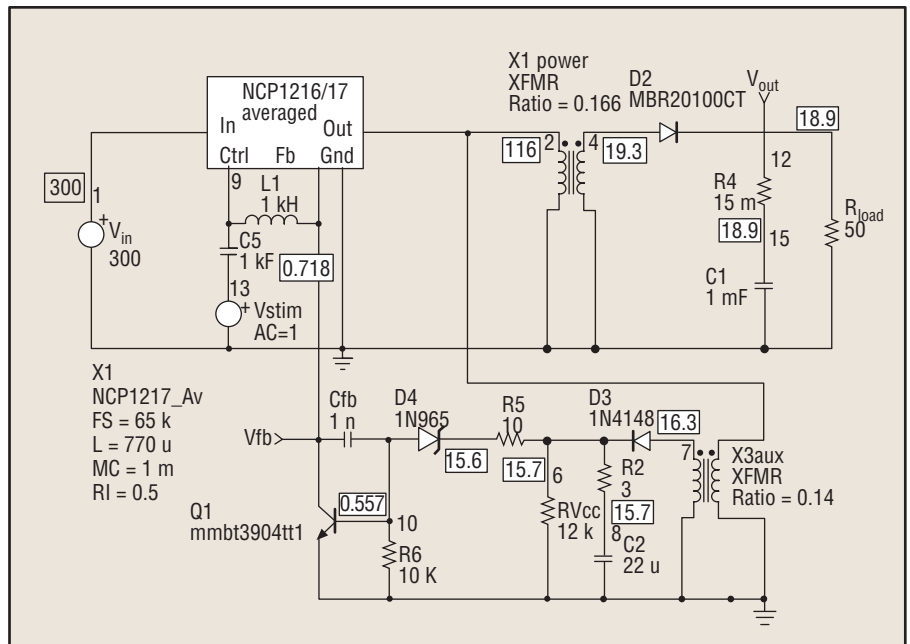


Fig. 7a. The complete average model implementing the NCP1217 model.

cost bipolar element Q1. This transistor is necessary because the feedback level must go down to reduce the amount of delivered power. The regulation point is actually D4's anode, the feedback (FB) point, loaded by the circuit Vcc pin.

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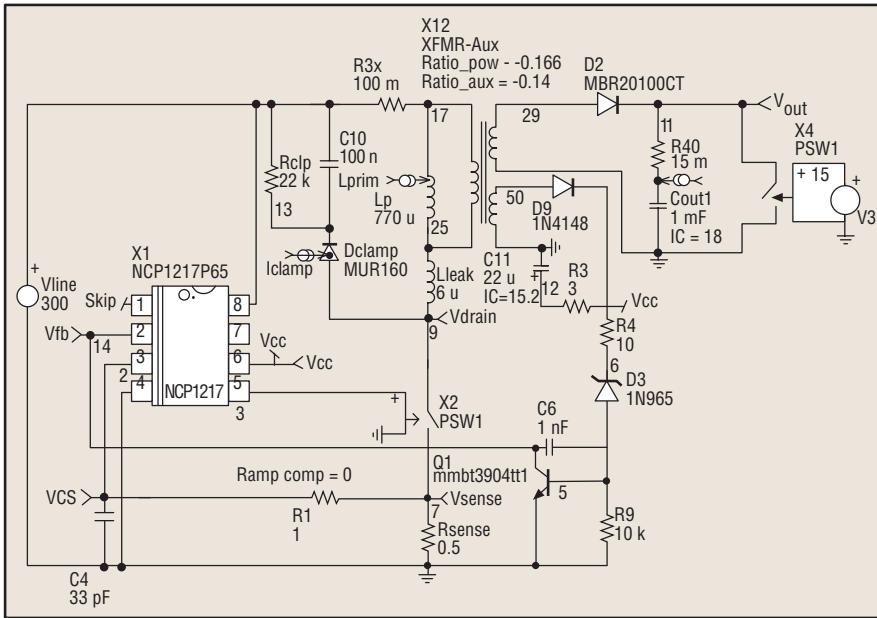


Fig. 7b. A cycle-by-cycle model helps validate the average approach.

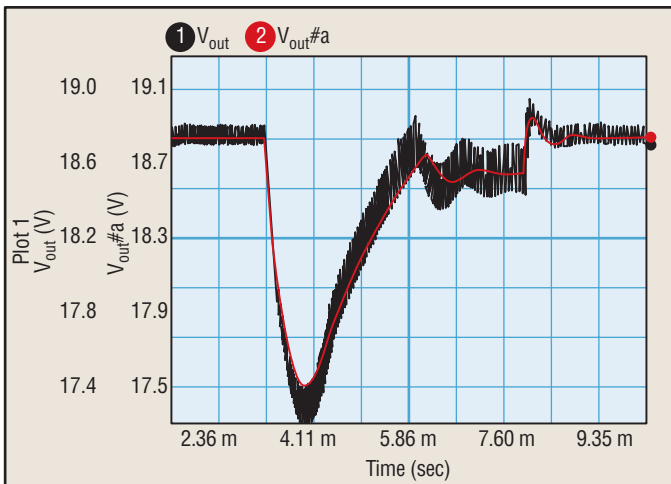


Fig. 7c. Average response (2) and transient cycle-by-cycle response (1).

The exercise will first consist in reflecting all secondary elements to the primary side, reducing the converter to a single output version. By using the simplified equations described previously, we can easily derive the drawing shown in Fig. 6b. The load is reflected as is the controller's consumption, which acts like a resistive element over the FB point. Also, during this reflective process, we consider the dynamic resistor of D1 and D3 close to zero.

To derive the first intermediate step depicted in Fig. 6b:

- Reflect the 4-Ω load to the auxiliary winding:  $4 \Omega \times (0.15/0.166)^2 = 3.26 \Omega$
- Reflect the output capacitor to the auxiliary winding:  $1 \text{ mF} \times (0.166/0.15)^2 = 1.22 \text{ mF}$ .
- Add the chip's power consumption via a simple resistor:  $12 \text{ V}/1 \text{ mA} = 12 \text{ k}\Omega$ .
- Combine capacitors and ESR together because both time constants are close:  $R7//\text{ResrEq}, \text{CeQout} + C5$  and  $R\text{VccEq}/\text{RloadEq}$ .
- Update the schematic as Fig. 6c shows.

From the final reflection, we can now locate the pole and zero, typical of a flyback converter operated in the discontinuous conduction mode (DCM):

$$Fp1 = \frac{1}{\pi \times \text{RloadTot} \times \text{CeQ}}$$

$$Fz1 = \frac{1}{2 \times \pi \times \text{Resr} \times \text{CeQ}}$$

Note that Rload can be derived in a simpler manner. Given the turn ratios, a 12-V output will imply a  $12 \times (0.15/0.166) = 10.84\text{-V}$  feedback voltage. If we deliver 3 A on the output, it corresponds to 36 W of power. From the auxiliary/FB level, it becomes an equivalent load of:  $P = V^2/R$  or  $\text{Req} = 10.84^2/36 = 3.26 \Omega$ .

## Where SPICE Helps

Thanks to an average SPICE model, testing the SMPS stability becomes child's play. There's no need to reflect capacitors, loads, resistors and so on or to adjust the paralleled combinations—SPICE does it for you automatically. For our case, we need to gather the flyback stage model (current or voltage mode) and then assemble the transformer configuration through the schematic capture.

Our Fig. 6a model thus will become Fig. 7a simulation circuit. Then, by installing a switch on the output and step loading it, we can check the stability of the power supply. Also, we can verify this average configuration by comparing the results delivered by a cycle-by-cycle simulation. Fig. 7b illustrates the cycle-by-cycle circuit, equivalent to Fig. 7a average model.

In this circuit, the power MOSFET has been replaced by a behavioral switch to speed the simulation time. By observing the output voltage when the switch is activated, we can compare the transient response of the average model and the cycle-by-cycle application. Fig. 7c shows both results and confirms the good matching between the average results and the transient model.

This article has shown the importance of running a comprehensive stability analysis of your switch-mode converter, including parasitic elements such as the output diodes dynamic resistance. Failure to do so will lead to major errors in the prediction of the poles and zeroes loci.

Also, when the converter gains in complexity (for example, with the addition of secondary-side inductive filters) the traditional hand analysis becomes complicated and tedious. Fortunately, SPICE offers the necessary flexibility to let you arrange the simulation template to match the real circuit and smoothly run an ac analysis, taking care of reflections and dynamic resistances for you. PETech

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