

Active Clamp Transformer Reset: High or Low Side?

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The choice of where to apply the active clamp transformer reset technique results in subtle differences in circuit implementation, affecting factors such as the value and voltage rating of the clamp capacitor, as well as the requirements for gate drive circuitry.

The active clamp transformer reset technique offers many well-documented advantages over traditional single-ended reset techniques, including lower voltage stress on the main MOSFET, the ability to switch at zero voltage, reduced EMI and duty cycle operation above 50%. Although the single-ended forward converter is undeniably the most popular power topology using the active clamp, the same advantages can be applied to flyback converters.

Numerous publications have compared the performance advantages of the active clamp over the more widely used RCD clamp, third winding and resonant reset techniques. However, there are application-specific design considerations of how to best apply the active clamp for optimal circuit performance.

All papers written on the active clamp technique show the clamp circuit applied to either the high side directly across the transformer primary or the low side directly across the drain-to-source of the main MOSFET switch. Even more interesting, the authors seem to be equally divided as to which application—high side or low side—is best, while offering little or no explanation as to why.

There are subtle but noteworthy differences between applying the active clamp transformer reset technique to the high side and applying it to the low side. Each application results in a different transfer function, which in turn results in different voltages applied to the clamp circuit during reset. The value and voltage rating of the clamp capacitor is directly affected, as well as distinct considerations between gate drive circuitry for each case.

Low-Side Clamp

Fig. 1 shows a low-side clamp applied to a basic single-ended forward converter with a standard full-wave rectified output and LC filter. Whenever the main MOSFET,

Q1, is conducting, the full input voltage is applied across the transformer magnetizing inductance. This is referred to as the power transfer mode.

Conversely, whenever the auxiliary (AUX) MOSFET, Q2, is conducting, the difference between the clamp voltage and the input voltage is applied across the transformer magnetizing inductance. This is referred to as the transformer reset period. Specific to the low-side clamp is the fact that the auxiliary MOSFET, Q2, must be a P-channel device only because of the direction of the body-diode.

Also note Q2 carries only the transformer magnetizing current, which has a very small average value compared to the reflected load current. For this reason, specifying a low gate charge MOSFET should be a primary consideration, with low $R_{DS(ON)}$ being only a secondary concern.

An additional dead-time period is introduced between the turn on and turn off transitions of Q1 and Q2. During the dead-time, primary current flow remains continuous through the body-diode of either the P-channel AUX MOSFET, Q2, or the main MOSFET, Q1. This is commonly known as the resonant period in which the conditions are set for zero voltage switching (ZVS). Although this is an important and unique characteristic of the active clamp topology, it's of little importance for this comparison, other than it always exists whether the active clamp is applied to the low side or the high side.

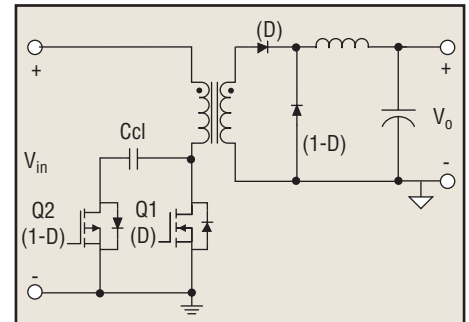


Fig. 1. Low-side active clamp circuit.

Neglecting the effect of leakage inductance, the transfer function for the low-side clamp can be derived by applying the principle of volt-seconds balance across the transformer magnetizing inductance.

$D \times V_{IN} = (1 - D) \times V_{C(LS)} - (1 - D) \times V_{IN}$ (1)
where D is the duty cycle, V_{IN} is the input to the clamp circuit, and $V_{C(LS)}$ is the clamp voltage. Simplifying (1) for the clamp voltage gives:

$$V_{C(LS)} = \left[\frac{1}{1 - D} \right] \times V_{IN} \quad (2)$$

Note that the transfer function given in (2) is also the same transfer function for a nonisolated boost converter, and this is why the low-side clamp is commonly referred to as a boost-type clamp.

The result of (2) gives an expression for the transfer function between the input voltage and the clamp voltage. However, notice from Fig. 1 that whenever Q2 is conducting, the clamp voltage is applied directly across the drain-to-source junction of Q1 and not the transformer primary magnetizing inductance. Therefore, (2) can be extended and written to include an expression for determining the drain-to-source voltage stress on the main MOSFET, Q1:

$$V_{DS(LS)} = V_{C(LS)} = \left[\frac{1}{1 - D} \right] \times V_{IN} \quad (3)$$

During the transformer reset period, the dot polarity on the transformer primary reverses, so the voltage applied to the primary is now defined as:

$$V_{RESET(LS)} = V_{C(LS)} - V_{IN} \quad (4)$$

If the expression for $V_{C(LS)}$ from (2) is substituted into (4) and simplified, a transfer function relating the input voltage to the reset voltage can be shown as:

$$V_{RESET(LS)} = \left[\frac{D}{1 - D} \right] \times V_{IN} \quad (5)$$

Furthermore, the duty cycle, D , of a single-ended forward converter is defined as the ratio of the output voltage to the input voltage multiplied by the transformer turns ratio, N .

$$D = \left[\frac{V_O}{V_{IN}} \right] \times N \quad (6)$$

Substituting (6) into (3) and (5) and simplifying gives expressions for $V_{DS(LS)}$ and $V_{RESET(LS)}$ in terms of V_{IN} , V_O and N , as shown in (7) and (8).

$$V_{DS(LS)} = V_{C(LS)} = \frac{V_{IN}^2}{V_{IN} - N \times V_O} \quad (7)$$

$$V_{RESET(LS)} = \frac{V_O \times V_{IN} \times N}{V_{IN} - N \times V_O} \quad (8)$$

The results of (7) and (8) now can be used to graphi-

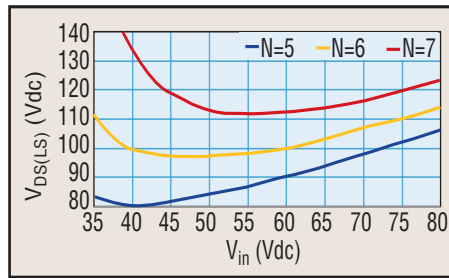


Fig. 2. MOSFET drain-to-source voltage stress for low-side clamp applied in a forward converter.

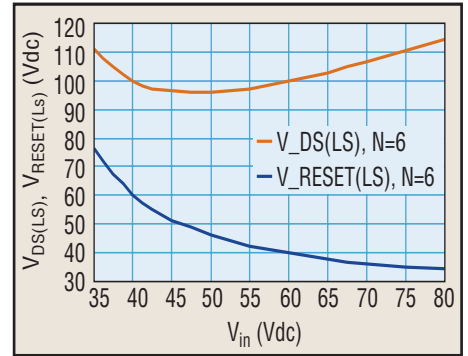


Fig. 3. Drain-to-source voltage stress and reset voltage for low-side clamp applied in a forward converter.

cally show how the clamp voltage and

transformer reset voltage vary with input voltage for a fixed value of V_O and a fixed transformer turns ratio, N . Using a value of 4 V for V_O (3.3 V plus some additional voltage drop), the graphical results of (7) are first plotted in Fig. 2 and shown for various transformer ratios, N .

From Fig. 2, notice the drastic variation in MOSFET voltage stress during minimum input voltage (maximum duty cycle, D). For this reason, a PWM controller, such as the UCC2891 shown in Fig. 4, must provide the capability of precisely limiting the maximum duty cycle. The consequence could be destructive voltage levels applied to the MOSFET or having to over specify the maximum MOSFET voltage rating.

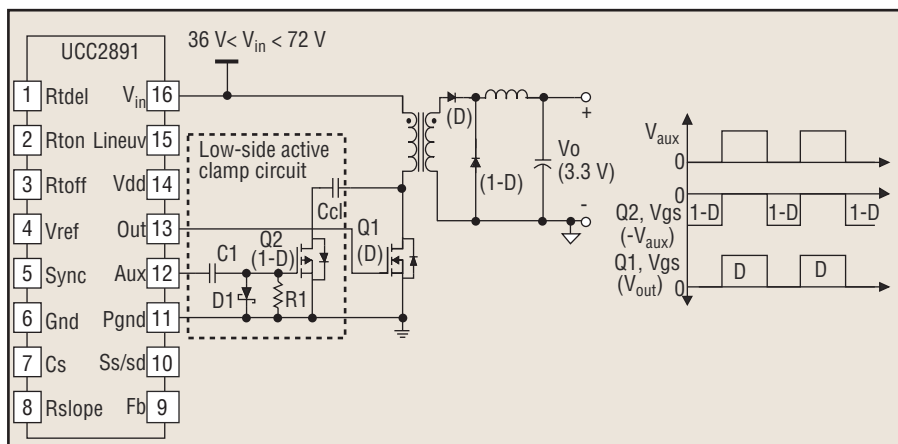


Fig. 4. Low-side clamp and gate drive circuit.

From an active clamp design standpoint, it's helpful to begin the power stage design by plotting the graph shown in Fig. 2. A transformer turns ratio can then be selected to yield a relatively constant $V_{DS(LS)}$ at each of the input voltage extremes. Fig. 2 shows that, for a typical forward converter operating over the full telecom input voltage ($36\text{ V} < V_{IN} < 75\text{ V}$), a turns ratio of $N = 6$ results in 110 V of applied drain-to-source voltage at $V_{IN} = 36\text{ V}$ and $V_{IN} = 75\text{ V}$.

The MOSFET voltage shown in Fig. 2 also is the voltage seen by the clamp capacitor, C_{cl} . As such, the clamp capacitor must be appropriately chosen to withstand the full clamp voltage plus any additional derating voltage. Having chosen a turns ratio of 6, the transformer reset voltage, $V_{RESET(LS)}$, given by (8) also can be plotted against varying input voltage (Fig. 3).

Gate Drive Considerations for Low-Side Clamp

Because it has already been established that the auxiliary MOSFET of a low-side clamp circuit must be a P-channel device, a negative gate drive voltage is required to turn this device on fully. However, most pulse-width modulator (PWM) controllers or gate drive ICs don't produce output-voltage levels below ground reference. Using a gate drive circuit applied to a low-side clamp, such as the one shown in Fig. 4, the P-channel MOSFET can

be directly driven from a low-side referenced driver or PWM gate drive signal.

Whether derived directly from a PWM or from a gate driver IC, the gate-to-source voltage of Q1, V_{OUT} , must be synchronously in phase with V_{AUX} , as shown in the timing diagram (dead-time delays not shown) of Fig. 4. Using an advanced PWM controller such as the UCC2891 simplifies the task of driving both MOSFET switches. Along with an internal $\pm 2\text{-A}$ drive, user-programmable dead time and a precise maximum-duty-cycle clamp, the UCC2891 provides the exact phasing and control specifically intended for low-side active clamp applications.

The first time the PWM gate voltage, V_{AUX} , goes positive, the diode, D1, will be forward biased and the capacitor, C1, will be charged to $-V_{AUX}$ volts. The capacitor voltage then discharges through R1. If the time constant of R1 and C1 (see Equation 9 and Fig. 4) is much greater than the PWM period, then the voltage across C1 remains relatively constant and the resultant gate to source voltage seen at Q2 is $-V_{AUX}$ with a peak positive value of zero volts. Therefore, V_{AUX} is effectively shifted below ground and is now adequate for driving the gate of the P-channel MOSFET, Q2.

$$R1 \times C1 \cong \frac{100}{F_{PWM}} \quad (9)$$

where F_{PWM} is the switching frequency.

Parameter	High-Side Clamp	Low-Side Clamp
V_{DS}	$\left[\frac{1}{1-D}\right] \times V_{IN}$	$\left[\frac{1}{1-D}\right] \times V_{IN}$
V_{RESET}	$\left[\frac{D}{1-D}\right] \times V_{IN}$	$\left[\frac{D}{1-D}\right] \times V_{IN}$
V_C	$\left[\frac{D}{1-D}\right] \times V_{IN}$	$\left[\frac{1}{1-D}\right] \times V_{IN}$
C_{cl} (applied voltage)	<ul style="list-style-type: none"> • Lower voltage by V_{IN} volts • Highest V_{cl} occurs at D_{MAX} • Careful attention for wide V_{IN} applications 	<ul style="list-style-type: none"> • Higher voltage by V_{IN} Volts • Transformer turns ratio critical at for limiting V_{cl} • Careful attention for high-voltage dc-dc applications
C_{cl} (component value)	• Same value as low side for given ripple voltage	• Same value as high side for given ripple voltage
AUX MOSFET	N-Channel	P-Channel
Gate Drive	<ul style="list-style-type: none"> • Gate drive transformer required • AUX MOSFET V_{GS} out of phase with main MOSFET V_{GS} – UCC2893 PWM controller 	<ul style="list-style-type: none"> • Simple RCD clamp gate drive • AUX MOSFET V_{GS} in phase with main MOSFET V_{GS} – UCC2891 PWM controller

Table. High-side clamp, low-side clamp comparison.

High-Side Clamp

Fig. 5 shows a high-side clamp applied to the same basic single-ended forward converter shown in Fig. 1. Similar to the low-side clamp, whenever the main MOSFET, Q1, is conducting, the full input voltage is applied across the transformer magnetizing inductance, which is referred to as the power transfer mode. Whenever the auxiliary MOSFET, Q2, is conducting, the clamp voltage, $V_{C(HS)}$ is applied directly across the transformer magnetizing inductance, referred to as the transformer reset period. This is quite different than the low-side case where the clamp voltage, $V_{C(LS)}$, was applied directly across the drain-to-source junction of the main MOSFET.

The high-side clamp auxiliary MOSFET, Q2, must be an N-channel device only because of the direction of the body-diode. Similar to the low-side clamp circuit, the dominant losses in Q2 are gate charge and switching losses; thus, a MOSFET is chosen with the same low-gate-charge considerations in mind.

Neglecting the effect of leakage inductance, the transfer function for the high-side clamp can be derived, once again, by applying the principle of volt-seconds balance across the transformer magnetizing inductance.

$$D \times V_{IN} = (1-D) \times V_{C(HS)} \quad (10)$$

Simplifying (10) for the clamp voltage, $V_{C(HS)}$, gives:

$$V_{C(HS)} = \left[\frac{D}{1-D}\right] \times V_{IN} \quad (11)$$

Note that the transfer function given in (11) is the same transfer function for a nonisolated flyback converter, which is why the high-side clamp is commonly referred to as a flyback-type clamp.

The result of (11) gives an expression for the transfer function between the input voltage and the clamp voltage. However, notice from Fig. 5 that whenever Q2 is conducting, the clamp voltage is applied directly across the transformer primary magnetizing inductance. Therefore, (11) can be extended and written to include an expression for determining the reset voltage:

$$V_{RESET(HS)} = V_{C(HS)} = \left[\frac{D}{1-D}\right] \times V_{IN} \quad (12)$$

During the transformer reset period, the dot polarity on the transformer primary reverses, so the voltage applied to drain-to-source of the main MOSFET, Q1, can be written as:

$$V_{DS(HS)} = V_{IN} + V_{C(HS)} \quad (13)$$

If the expression for $V_{C(HS)}$ from (11) is substituted into (13) and

simplified, a transfer function relating the input voltage to the main MOSFET drain-to-source voltage can be shown as:

$$V_{DS(HS)} = \left[\frac{1}{1-D}\right] \times V_{IN} \quad (14)$$

Substituting (6) into (12) and (14) and simplifying gives expressions for $V_{RESET(HS)}$ and $V_{C(HS)}$ in terms of V_{IN} , V_O and N , as shown in (15) and (16).

$$V_{RESET(HS)} = V_{C(HS)} = \frac{V_O \times V_{IN} \times N}{V_{IN} - N \times V_O} \quad (15)$$

$$V_{DS(HS)} = \frac{V_{IN}^2}{V_{IN} - N \times V_O} \quad (16)$$

The results of (15) now can be used to graphically show how the clamp voltage and transformer reset voltage vary with input voltage for a fixed value of V_O and a fixed transformer turns ratio, N . Using the same previous value of 4 V for V_O (3.3 V plus some additional voltage drop), the graphical results of (15) are plotted in Fig. 6 and shown for various transformer ratios, N .

Since the MOSFET drain-to-source voltage given by (16) is identical to the low-side clamp, $V_{DS(LS)}$, given by (7), the graphical result for (16) can also be represented by Fig. 2.

Gate Drive Considerations for High-Side Clamp

Unlike the low-side clamp circuit

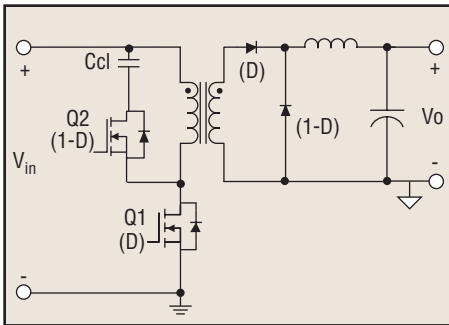


Fig. 5. High-side active clamp circuit.

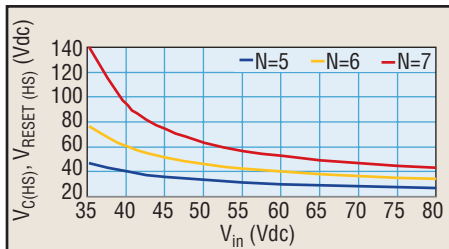


Fig. 6. Clamp voltage and reset voltage for high-side clamp applied in a forward converter.

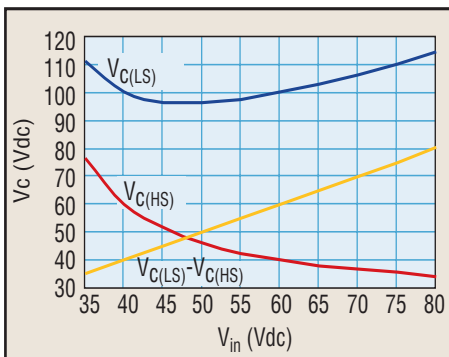


Fig. 7. Comparison of high-side versus low-side clamp voltages.

of Fig. 4, the high-side clamp makes use of an N-channel auxiliary MOSFET. Assuming the PWM controller doesn't have an internal high-side driver stage, a 1:1 gate drive transformer configured as shown in Fig. 8 can be used. For high-side active clamp circuits, the gate-to-source voltage of Q1, V_{OUT} , must be asynchronously out of phase with V_{AUX} , as shown in the timing diagram (dead-time delays not shown) of Fig. 8.

The UCC2893 active clamp PWM controller is electrically and functionally equivalent to the UCC2891 shown in Fig. 4 with one exception: where the UCC2891 is intended for low-side active clamp circuits, the UCC2893 provides the exact phasing and control specifically intended for high-side ac-

tive clamp applications. Therefore, the V_{AUX} output of the UCC2893 is out of phase with the V_{OUT} output, as shown in the timing diagram of Fig. 8.

Clamp Capacitor Selection

Whether using a high-side or low-side active clamp circuit, the volt-seconds applied to the transformer primary must balance, making the transformer reset voltage equal for each

case. And because the primary MOSFET drain-to-source voltage stress and transformer reset voltage are the same for each circuit, it's the varying clamp voltage applied across the clamp capacitor, C_{cl} , that must be considered. The details of the clamp capacitor voltage variations can be seen by comparing the difference between the clamp voltage transfer functions for each case.

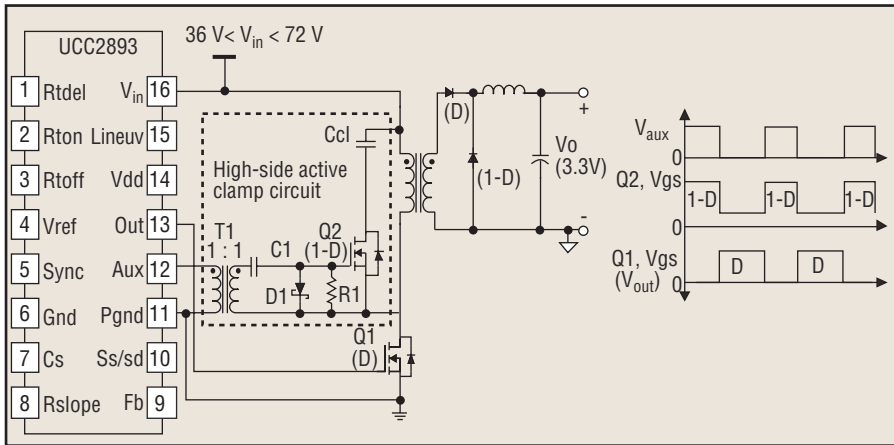


Fig. 8. High-side clamp and gate drive circuit.

$$\Delta V_c = V_{C(LS)} - V_{C(HS)} \quad (17)$$

Substituting (2) and (11) into (17), ΔV_c can be written as:

$$\Delta V_c = \left[\frac{1}{1-D} \right] \times V_{IN} - \left[\frac{D}{1-D} \right] \times V_{IN} = V_{IN} \quad (18)$$

The result of (18) shows that $V_{C(LS)}$ is greater than $V_{C(HS)}$ by V_{IN} volts. Considering the range of V_{IN} to be $36\text{ V} < V_{IN} < 72\text{ V}$, a graphical comparison of $V_{C(HS)}$, $V_{C(LS)}$ and ΔV_c is shown in Fig. 7.

Therefore, the first consideration for sizing the clamp capacitor is to know what the appropriate voltage rating should be over a given range of V_{IN} . The graph in Fig. 7 shows that ΔV_c linearly increases with V_{IN} . For higher values of V_{IN} , the high-side clamp offers the lowest voltage stress. However, the capacitor must still be selected based upon the rising clamp voltage seen at minimum V_{IN} , maximum D , which is about 80 V for this example.

The value of the clamp capacitor primarily is chosen based on the amount of allowable ripple voltage that can be tolerated. Also, it's assumed the value of the capacitor is large enough to approximate the clamp voltage as a constant voltage source. However, according to (2) and (11) V_{cl} changes with input voltage.

Whenever a line transient or sudden change in duty cycle is commanded, it takes a finite amount of time for the clamp voltage, and therefore the transformer reset voltage, to

adapt. Larger capacitor values result in less voltage ripple but introduce a transient response limitation. Smaller capacitor values result in faster transient response, at the cost of higher voltage ripple.

Ideally, the clamp capacitor should be selected to allow some voltage ripple, but not so much as to add additional drain-to-source voltage stress to the main MOSFET, Q1. Allow approximately 20% voltage ripple while paying close attention to V_{DS} of Q1.

ing C_{cl} in terms of known design parameters:

$$C_{cl} > \frac{10 \times (1 - D_{min})^2}{L_{mag} \times (2 \times P \times F)^2} \quad (20)$$

Once C_{cl} is calculated by (20), the final design value may vary slightly after the clamp capacitor ripple voltage is measured in circuit. Furthermore, (20) is valid for both the high-side and low-side active clamp circuit. Thus, for a desired clamp ripple voltage, the clamp capacitor component value will be the same for each case.

There are similarities as well as subtle but important differences between applying the active clamp circuit to the high side versus the low side. A direct comparison between the differences and similarities is summarized for each circuit in the table.

The drain-to-source voltage stress, V_{DS} , on the main MOSFET and the transformer reset voltage, V_{RESET} , are the same for both circuits. The differences between the clamp voltage transfer functions may seem minor, but each has a significant effect on the

For single-ended power converter applications requiring the absolute lowest voltage stress on the clamp circuit, the high-side clamp is the best choice.

A simplified method for approximating C_{cl} , is to solve for C_{cl} , such that the resonant time constant is much greater than the maximum off-time. Although additional factors such as the power stage time constant and control loop bandwidth also affect transient response, this approach, stated in (19), assures transient performance isn't compromised—at least from the active clamp circuit point of view.

$$2 \times P \times \sqrt{L_{mag} \times C_{cl}} > 10 \times t_{OFF(MAX)} \quad (19)$$

where L_{mag} is transformer magnetizing inductance and $t_{OFF(MAX)}$ is the maximum off-time.

By dividing both sides of (19) by the total period, T , and solving for C_{cl} , (19) can be rewritten as (20), express-

clamp capacitor selection and transformer turns ratio.

For single-ended power converter applications requiring the absolute lowest voltage stress on the clamp circuit, the high-side clamp is the best choice. Even though the high-side clamp produces a lower overall clamp voltage, the voltage tends to rise more sharply at minimum V_{IN} , maximum duty cycle. Therefore, specific attention must be paid to accurately limit the maximum allowable duty cycle so that the maximum V_{DS} of the main MOSFET isn't exceeded.

The high-side clamp uses an N-channel AUX MOSFET, so more component choices are available than the low-side clamp using a P-channel device. However, the high-side clamp

circuit requires a gate drive transformer, which may come into play when absolute low cost is a primary concern.

Compared to the high-side counterpart, the low-side clamp yields a slightly higher but better controlled clamp voltage when the transformer turns ratio is properly selected, according to Fig. 2. The gate drive circuit for the low-side clamp AUX MOSFET also is simpler, because a gate drive transformer isn't required. When the input voltage range is 2:1 or greater, the low-side clamp is a good choice, because a higher duty cycle can be tolerated with less variation in clamp voltage.

Whether a high-side or low-side clamp is applied, the efficiency and performance benefits are huge compared to the better-known RCD clamp and resonant reset techniques. With the advantage and flexibility of advanced PWM controllers, such as the UCC2891 family, the complexities normally with implementing active clamp transformer reset are greatly simplified. PETech

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