

# Power-Monitoring Circuits for Battery Performance

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Simple IC-based designs measure power to the system's loads by multiplying dc load currents and supply voltages.

**E**lectronic systems are often subject to the power limitations imposed by their power supplies and batteries, and the maximum power available from those sources often must be minimized to reduce the system's cost, size and weight. Exceeding the maximum power limit can lead to shortened battery life or power-supply failure. Therefore, it is important that the power demand remain below a specified threshold.

One way to limit the amount of power supplied to a load is to monitor load current with a current-sense amplifier. The effective power is then proportional to the sensed current, provided the source voltage is known and constant. This technique is adequate for many applications, but others require true power monitoring. For those, you

must monitor power consumed by the load directly. Examples include battery-driven applications, in which the cell voltages change with respect to time.

In addition to detecting power-limit thresholds, power monitoring can arbitrate the amount of power allocated to selected subsystems, according to the total power required at that moment by the system. By allowing the use of smaller power supplies and batteries for a given application, this approach further reduces the size, cost and weight of the battery and the system.

DC power monitoring is conceptually straightforward, simply multiply the monitored dc load current by the measured dc supply voltage. Actual implementations are more complex, however, because the accurate multiplication of analog signals is not trivial. One effective method of multiplication is accomplished by converting measured current information into the pulse-width of a PWM waveform, and converting measured voltage into the PWM waveform's height.

After low-pass filtering the PWM signal, the remaining dc level is proportional to power consumed by the load. The Fourier coefficients for a repetitive pulse sequence of duty cycle  $D$  and unit height are:

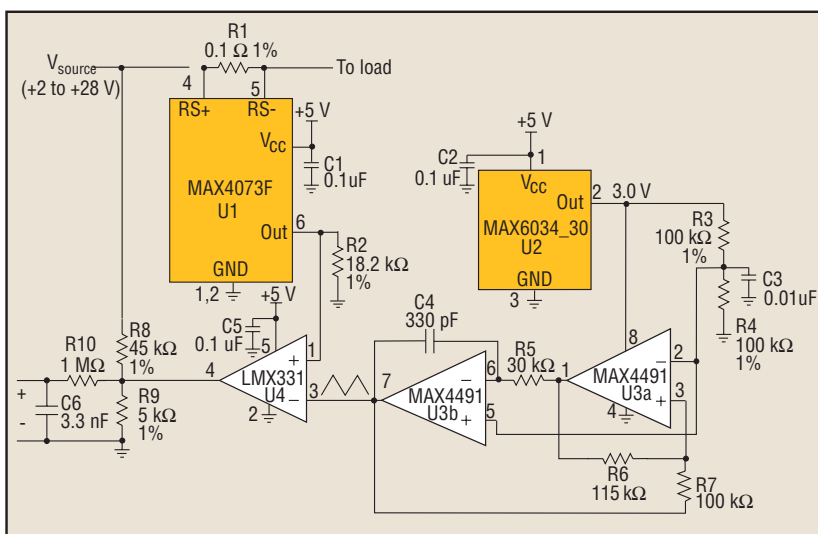
The Fourier coefficients for a repetitive pulse sequence of duty cycle  $D$  and unit height are:

$$P_n = \begin{cases} D, & n=0 \\ e^{-j\pi nD} \sin \pi nD, & n>0 \end{cases}$$

where  $n$  is the coefficient number. Low-pass filtering removes all ac components of the series, leaving only the dc term:

$$P_n = \begin{cases} D, & n=0 \\ \approx 0, & n>0 \end{cases}$$

To complete this analysis, incorporate the measured source voltage as the amplitude of the PWM waveform, and relate the PWM duty



**Fig. 1.** In this basic power monitor circuit, U1 generates a voltage that is proportional to the load current sensed through R1, while U2 and U3 create a supply independent triangle waveform.

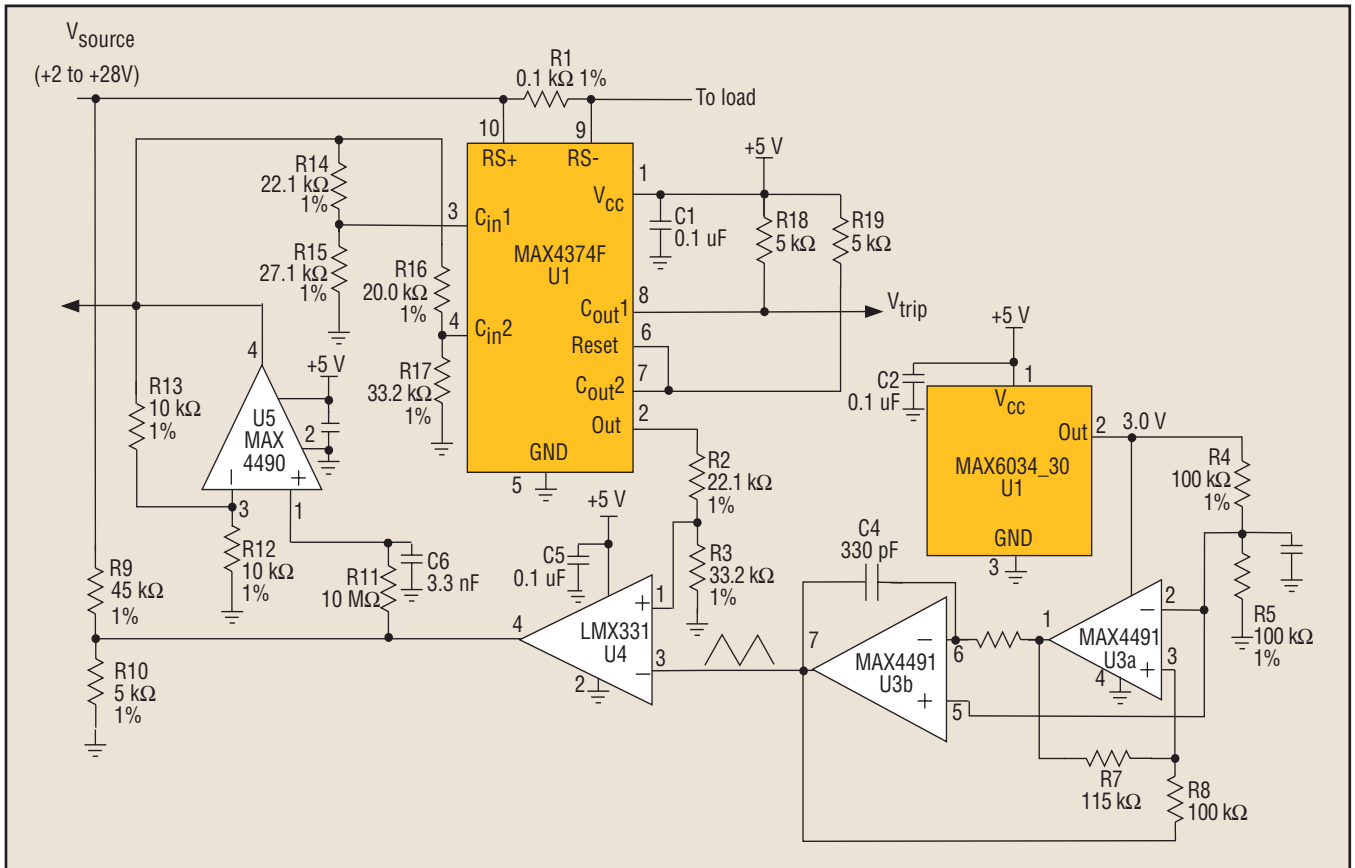


Fig. 2. The power-monitor circuit of Fig. 1 is enhanced by replacing U1 with the MAX4374.

cycle to load current. The dc output of the low-pass filter can then be expressed as:

$$P_{DC\_LPF} \approx (c_v V_{SOURCE}) D = (c_v V_{SOURCE}) \left( \frac{I_{LOAD}}{I_{MAX}} \right) = K (V_{SOURCE} I_{LOAD})$$

where  $c_v$  is a voltage-attenuation constant whose presence will be made obvious in subsequent application circuits,  $I_{MAX}$  is the maximum load current, D has been replaced by  $I_{LOAD}/I_{MAX}$ , and K is a scaling constant that relates measured source voltage and load current to the low-pass filtered output voltage. Note that source voltage is measured rather than load voltage. Source and load voltage are roughly equal, but a source-voltage measurement provides a more accurate representation of power consumed by the load and associated current-sense device.

In a basic implementation of the power-monitor circuit (Fig. 1), current passes from source to load through the current-sense resistor R1. In conjunction with R1, U1 provides an output voltage equal to  $R1 \cdot I_{LOAD}$ , which is five times the actual load current. Assuming a maximum sense voltage of 100 mV for U1 (and with R2 not present), this configuration implies a maximum sense current of 1 A and a corresponding U1 output voltage of 5 V. Incorporating R2 reduces the overall maximum output voltage to 3 V.

U2 and U3 create a supply-independent triangle waveform with limits close to 0 V and 3 V. U2 regulates the  $V_{CC}$  of U3 to 3 V, and U3 with its associated components form a well-known triangle-wave generator, whose

frequency of oscillation is given by:

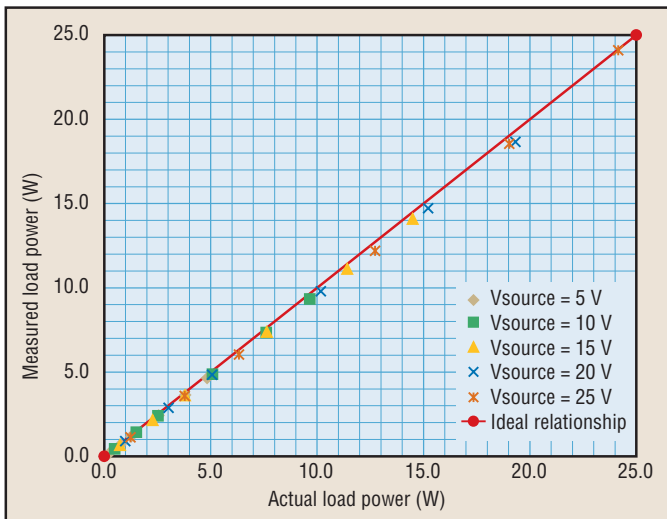
$$f_{OSC} = \frac{1}{4} \frac{R_6}{R_3 C_4 R_7}$$

The theoretical threshold limits of this waveform are  $V_{th-} = \alpha V_{CC2}$  and  $V_{th+} = (1-\alpha)V_{CC2}$ , where  $V_{CC2}$  is the triangle-waveform generator's 3-V supply, and  $\alpha$  is given by:

$$\alpha = \frac{R_6 - R_7}{2R_6}$$

Actual limits will differ slightly because of parasitic resistances. The triangle waveform generated by U3 is applied to the negative input of open-drain comparator U4, and the output from U1, now scaled to a maximum voltage of 3 V, is applied to the positive input of U4. U4's output is a PWM signal whose pulse width is proportional to current, and the signal's load-voltage portion is incorporated into the PWM circuit through the R8/R9 voltage divider, which sets the  $c_v$  values described previously. Because U4 has an open-drain output, the divider voltage sets the height of the PWM waveform. The values of these resistors were chosen to scale the load voltage by 0.1 while reducing the loading effect of R10. Finally, the PWM signal is low-pass filtered with R10 and C6, thereby creating a dc signal proportional to the consumed load power.

For an enhanced implementation of the basic power monitor (Fig. 2), the current-sense device (U1) has been replaced with a MAX4374F. Besides a current-sense am-



**Fig. 3.** Experimental data confirms a close correlation between measured power and actual power in the power-monitor circuits in Figs. 1 and 2.

plifier, this device includes two comparators and an internal reference, which allow the generation of flags based on certain power conditions. This circuit can be used for power-based circuit-breaker applications in which a series FET must be shut off during overpower conditions.

The second comparator lets you release the triggered over power condition when power levels have returned to acceptable levels (set by R16 and R17). An additional op amp (U5) and associated resistors have been added to

buffer the analog output voltage generated by the high-impedance low-pass filter.

As shown in Fig. 3, the circuits of Figs. 1 and 2 closely track the ideal relationship of  $P_{\text{MEASURED}} = P_{\text{ACTUAL}}$ . Further improvements in x-intercept accuracy can be achieved by decreasing  $\alpha$ , thereby forcing the triangle wave to approach its rails more closely. Take care to avoid saturating the triangle wave. Increased gain can be achieved by adjusting any of the resistors along the current-sense signal path.

Note that precision 1% resistors have been used to minimize the gain error. That measure is especially important for resistors along the signal path. In addition to gain error, other errors arise from U4's comparator offset and from aberrations in the triangle waveform (nonlinearity of the waveform slopes, waveform limits not exactly at the rails, and rounded waveform shapes at the maxima and minima).

Finally, remember there are other methods for performing the multiplication required for computing load power, including degenerated differential pairs (the Gilbert cell), log/anti-log amplification, and digital conversion and multiplication. In contrast, however, the circuits presented here offer relative simplicity, low cost and low power. PETech

### Acknowledgments

The author wishes to thank Miles Bekgran for his extensive lab work in support of this article.

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