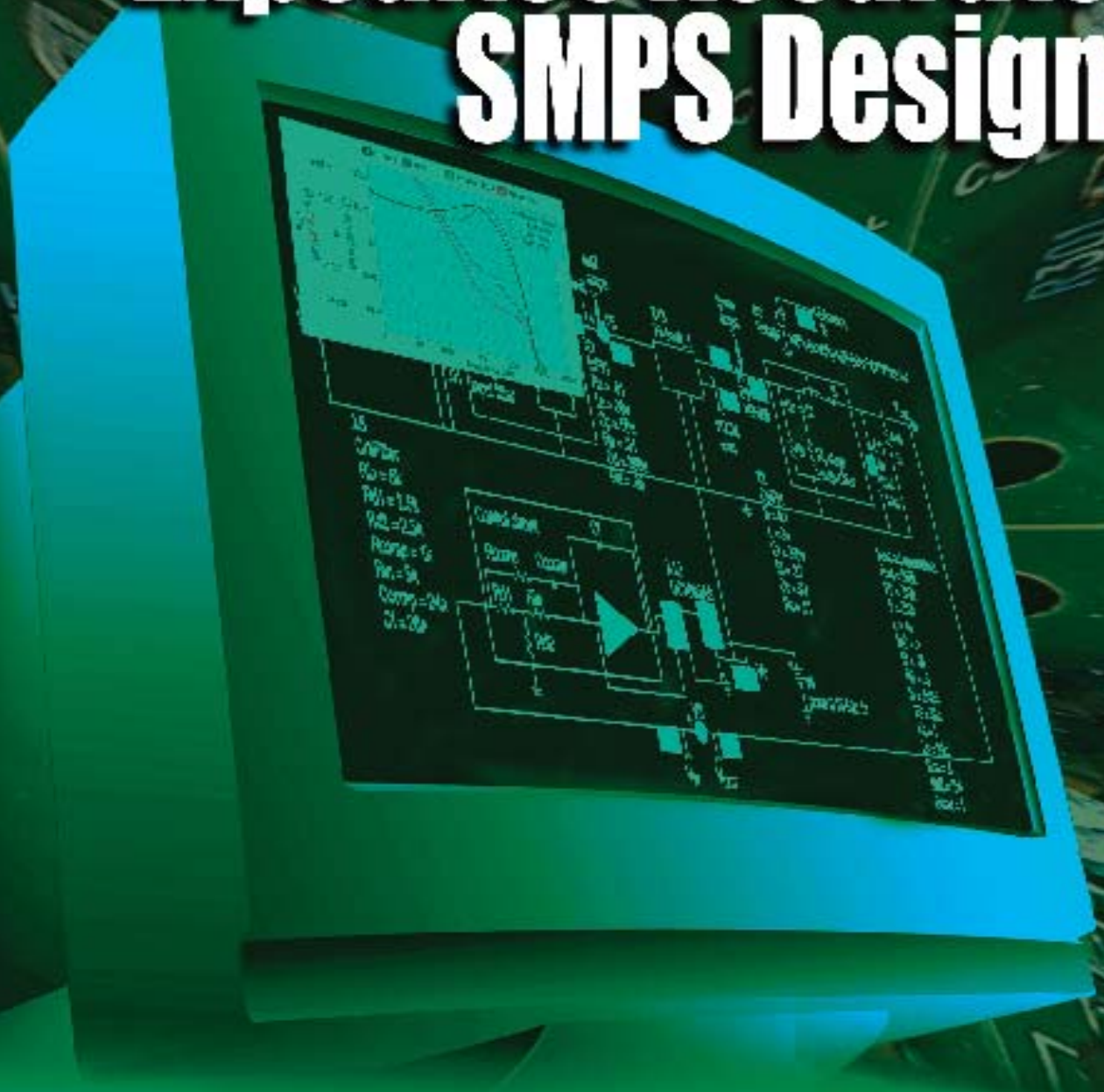


Ultra-Fast Simulation Expedites Accurate SMPS Design



A designer can put together a complete design before ordering the parts needed to build a prototype by using merely a desktop computer and some innovative SPICE software.

By Larry Meares, President, Intusoft, Gardena, Calif.

Today, clean power is a key concern. Switch-mode power supply (SMPS) makers strive to ensure their designs offer power that's as clean as possible. Many designs fail as a result of the inability to satisfy European and U.S. safety agency standards (i.e., electromagnetic compatibility and line transient requirements). The ubiquitous personal computer's characteristic cosine shaped power pulse, shown in Fig. 1, requires 75% more current carrying capacity than necessary. Moreover, the turn-on surge can be large enough to cause operational glitches in other equipment. Related considerations with SMPS, such as overshoot and component stress at power up; snubbing of loadline; and EMI, comprise many facets to SMPS development.

Advantages gained by using the latest applications provided by automated circuit design tools in meeting these criteria help speed the design process and improve product reliability. A designer can put together a complete design before ordering the parts needed to build a prototype. Today, the traditional breadboard is nearly obsolete because component geometries are becoming too small to manage practically using a lab paradigm. For instance, excessively large geometries from pins on breadboards create ca-

pacitive and inductive parasitics. This, in turn, would degrade the debugging of SMPS designs, which are particularly sensitive to such phenomenon.

As computers have become faster, so have modeling techniques used to simulate SMPS operation—including better convergence and accuracy. Specifically, software tools that address the design criteria of SMPS have advanced forward with analog and mixed-signal circuit simulation tool suites, while complete schematic templates include a wealth of power supply models. The combined tool ICAP/4 showcases actual parts in applications that fit the needs of power supply designers, while special provisions accommodate the ON Semiconductor power supply templates—all available in downloadable demo format.

A series of other new features in this simulation suite also provides important new benefits to the power supply designer. Examples include: large-signal average models; scripts for loop stability analysis; transformer and inductor design derived directly from SMPS electrical specifications; system level models for 60 Hz mains and SMPS loads; high frequency models for power capacitors and inductors; special injection models for measuring open loop properties within a closed loop circuit configuration; and automated extensions for

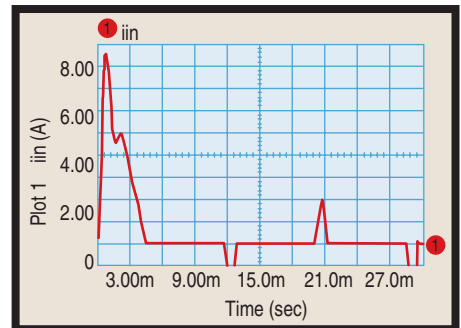


Fig. 1. Mains inrush current at turn-on and steady state cosine shaped current pulse. Peak repetitive current is nearly seven times greater than that of a power factor corrected circuit.

advanced waveform post-processing functions. This last feature permits the designer to quickly view any number of specialized wave functions such as EMI compliance for IEC line harmonics and high frequency conduction (i.e., specified in CSPR16 and MIL-STD-461). Another example includes EIC class A, B, C, and D specification waveforms compared with those produced by a design simulation.

Templates Enable Faster and More Automated Design

To give designers a quick start and faster solution, it includes a new power supply template technology. Consequently, the ICAP/4 offers generic forward and flyback converter topologies, plus more than 25 templates for ON Semiconductor products.

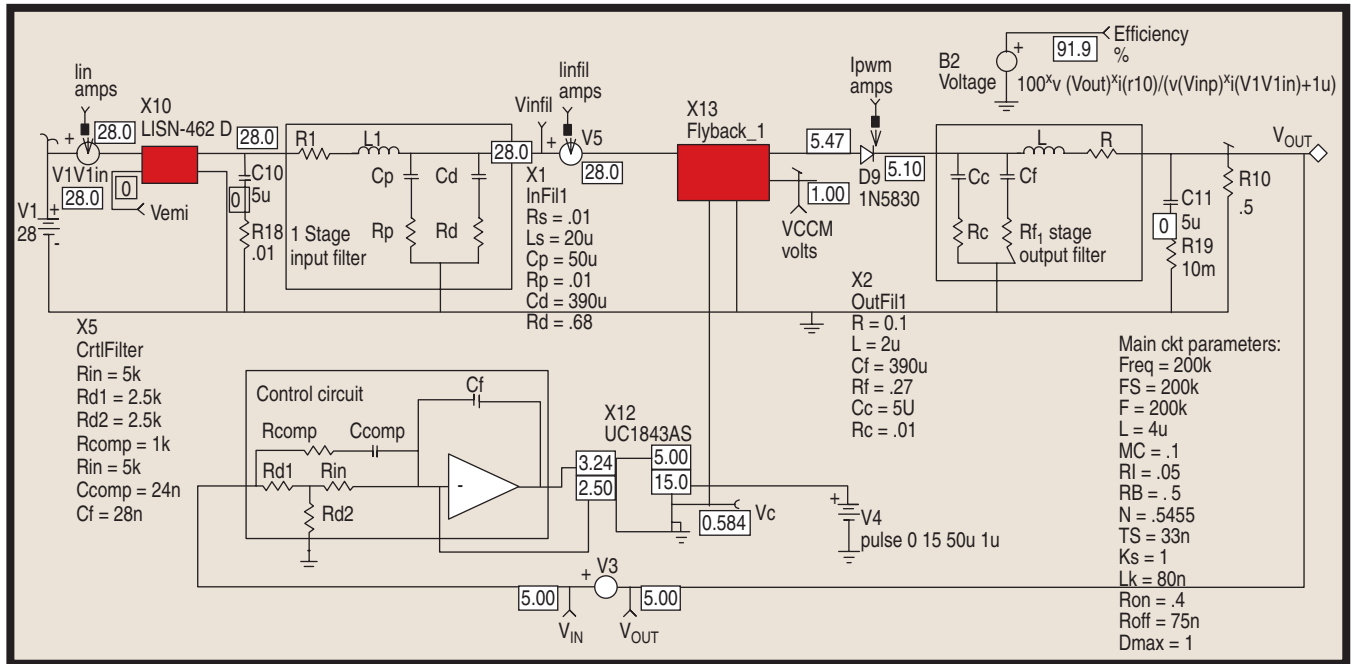


Fig. 2. A portion of a Flyback power supply template drawing, which helps you choose from many standard library blocks to build a power supply.

Fig. 2 contains the simulation tool's SpiceNet schematic entry system.

SpiceNet features layers (configurations) of different design overlays,

each maintaining a common core of circuitry and parts. A "FwdTemplate"

topology, for example, has special layers for the average, switching and hierarchical models. These layers are combined with common circuitry and test circuitry to create three unique drawings. A fourth configuration uses the switching model to observe transistor switching load-line, measure component transient stress, and calculate the circuit's EMI signature.

Power supply templates from the power library provide the standard blocks for power supply construction. Design simulations are then performed on the appropriate drawing topology, each embedded with the selected SMPS model into its hierarchy. The system allows the user push down into a desired model to measure internal properties like duty ratio, resistive dissipation, and dynamic dissipation. The designer will then rescale the blocks for his or her desired power and voltage levels.

Fig. 3 shows a portion of a Flyback

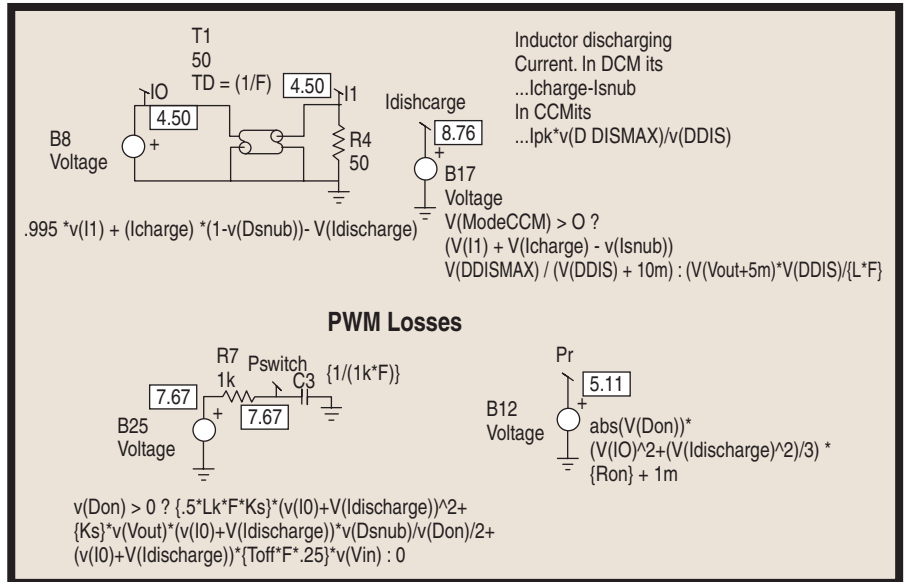


Fig. 3. Portion of a Flyback model showing losses. Notice that the internal power dissipation is broken down into resistive and switching components to provide visibility into the inductor current levels. You obtain this model by simulating the average schematic configuration.

model using the new average models in this schematic configuration. The internal power dissipation is broken

down into resistive and switching components to obtain the inductor current levels.



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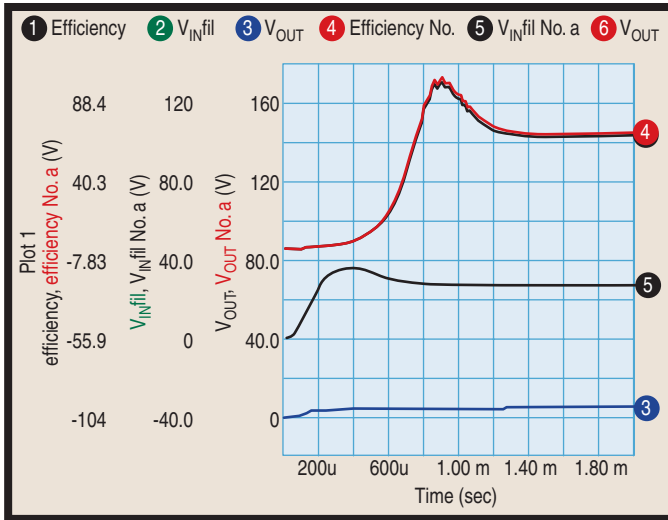


Fig. 4. The switched and average model results are almost exactly the same.

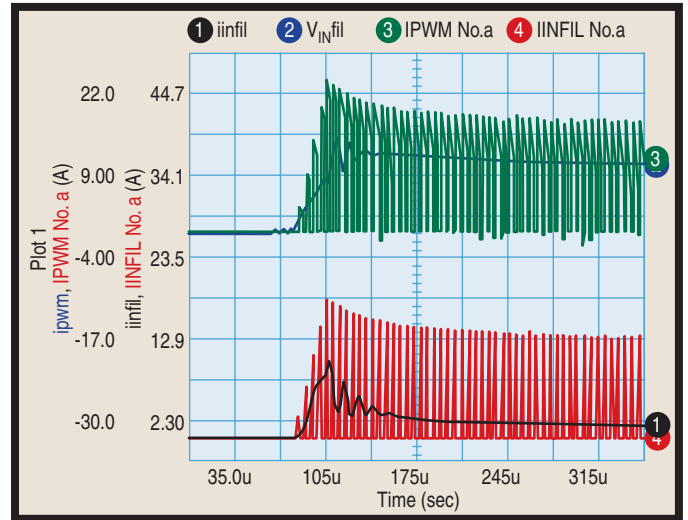


Fig. 5. Average model exposes turn-on instability.

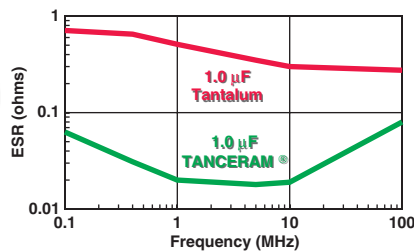
New Fast Average Models Provide Large-Signal Transient Response

Referring again to Fig. 2, on page 16, the design's average models are unique in several ways. First, they include PWM losses and sampling transport delay. Second, while providing traditional small signal analysis, they work for simulation of large signals where the results can be applied to

start-up and line/load sensitivities. Transient response eliminates the simulation of switching clutter. This serves to reveal large signal instability at turn on (minus slope compensation). Further, on start-up, loss as a percent of power input is much higher than steady state. They accurately replicate cycle-by-cycle switching simulations in a fraction of the time (100-fold faster). Also evolving from this vast increase in speed is the practicability of design optimization simulation technology in the time domain—what was prohibitively long in the past.

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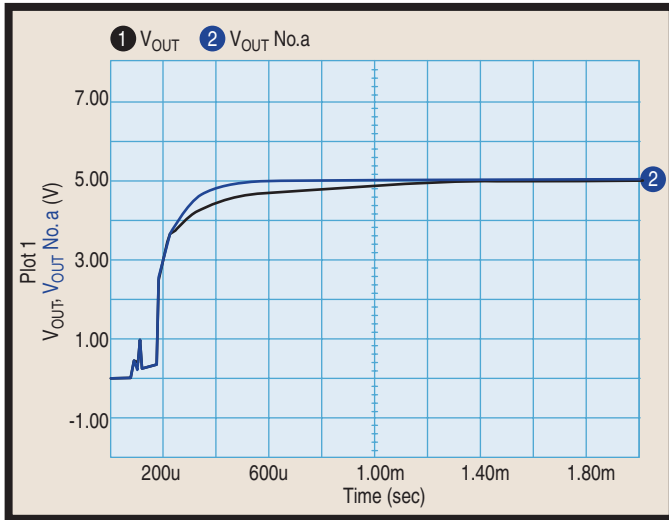


Fig. 6. Black waveform is before Optimization; blue, afterward.

such as gain and phase margin. The process is based on a general feedback theorem (GFT), devised by Dr. R. David Middlebrook with the California Institute of Technology. GFT provides a special nulling matrix that balances closed loop electrical properties by injecting a constant voltage and variable current at the cut point (injection point) in the design loop. Though difficult, this would be performed in hardware using complex signal generators (sine and cosine) to force the nulling condition at an insertion point.

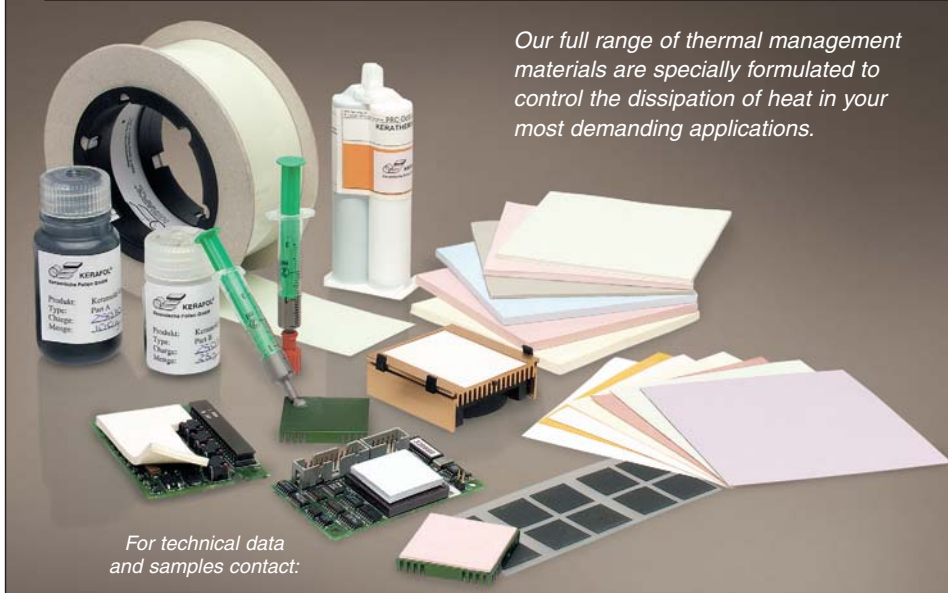
Optimizing Designs in the Time Domain

A power supply must have ample gain/phase stability margins, as measured using a Bode plot. Yet, the large signal behavior must also be constrained by start-up, and line/load variations. Finding the best component values for a design section is an important requirement. The optimizer does this by reducing the error between iterations performed by the optimizer until the most efficient set of component values is ascertained.

The large signal average model has enabled the SMPS control system to be optimized in the time domain. Fig. 6 shows the result of using time domain optimization to shape the design's control compensation for the best start-up characteristic. There are two parts to this objective function. First is to get to an accurate final condition after 400 usec. Next is to simultaneously penalize overshoot after 200 usec, which will generally lower bandwidth in favor of stability. Simulations and settings are assigned in dialog boxes within the simulation software. The algorithm used varies each parameter over its range and measures this in relation to the objective function. Reference simulation is run before optimization. After the optimization has finished, a final run is made, which provides before and after results for display.

To observe the effects of the gain and phase margins of the design example, the optimizer results are recorded. Successively, an "AvgSubckt + ac" analysis is run. Fig. 6 shows how the transient response, and gain and phase margins

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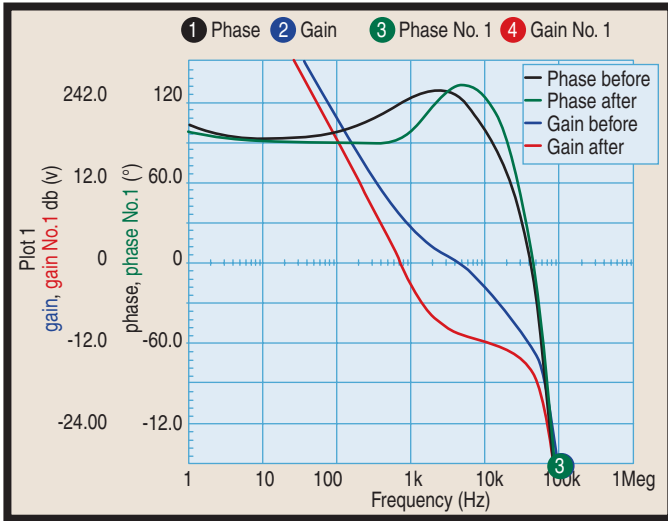


Fig. 7. Bode plot shows improved margins with optimization.
 Before: gain margin = 12.2282 db(V) phase margin = 123.491°.
 After : gain margin = 15.3280 db(V) phase margin = 85.7452°.

improve. Fig. 7 also displays V_{OUT} , V_{OUT} No. a (post optimization), phase, and phase No. 1 in degrees.

Clicking on ICAP/4's "EMI Standard" function from its waveform calculator performs a pre-existing script for the emission specification check, derived from the tool's unique

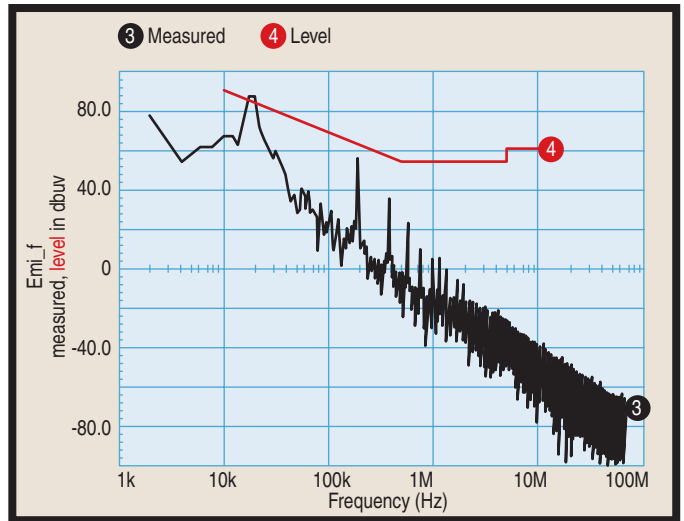


Fig. 8. EMI plot for Vemi.

SPICE script. The schematic configuration is from a "Tran-Subckt," with results displayed in Fig. 8.

These advantages are changing the way designers work. Using ultra-fast CAE software makes accurate SMPS designs possible in much less time than previously possible. **PETech**

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