

# Paradigm Shift in Planar Power MOSFET Technology

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New planar power JBSFET architecture increases dc-dc converter efficiency because of a dramatic improvement in the  $[R_{DS(on)} * Q_{GD}]$  figure-of-merit and the integration of a maximum current rated Schottky diode, within the power MOSFET cells to clamp-off the parasitic body diode.

**E**ach new generation of microprocessors has seen the integration of a larger number of transistors operating at higher clock frequencies with the goal of enabling higher performance in computing and graphics applications. The integration of more transistors on a chip is made possible by reducing their size using lithography with smaller feature dimensions. Because of the constraints dictated by the maximum electric field and power dissipation that can be tolerated by silicon, each microprocessor generation has been optimized to operate at lower voltages.

The larger number of transistors per chip, all operating at higher clock frequencies, has required an increase in the power consumed by each generation of microprocessor technology. This combination of increased power consumption at lower operating voltages has led to a dramatic increase in the power supply current.

**Limitations in the performance of the control and sync FETs are an important roadblock for achieving the desired power delivery to microprocessors with reasonable efficiency.**

sign is based on the sync-buck topology (Fig. 1). The input power supply voltage ( $V_{IN}$ ) is stepped down to the operating voltage needed by the microprocessor by controlling the duty cycle of the two power MOSFETs. In a typical 12-V power supply delivering power at an output voltage of 1.2 V, the duty cycle is 10%—with the control FET on for 10% of the time and the Sync FET on for 90% of the time during each period. As the power supply current required by the microprocessors has increased, it has been found that multiple phases of the sync-buck circuit are re-

The SIA roadmap indicates an operating voltage of 1.1 V with 170 A for microprocessors in 2005. High-performance voltage regulators that achieve these difficult targets are required to power future microprocessors.

The most commonly used voltage regulator de-

quired. In addition to reducing the current handling capability per phase, multiphase converters enable reduction of ripple current and improved efficiency at light loads by powering down phases.

However, rapid response to the power needs of the microprocessor require operation of each phase at higher switching frequencies. The current slew rates must be sufficiently high (more than 150 A/ $\mu$ s) for the voltage regulator to allow sections of the microprocessor to be rapidly shut down and reactivated for power savings. To achieve a response time of 5  $\mu$ s to 6  $\mu$ s, the multiphase converter must operate at a switching frequency of 1 MHz to 3 MHz per phase<sup>[1]</sup>.

Limitations in the performance of the control FET and sync FET have been identified as a roadblock to achieving the desired power delivery to microprocessors with reasonable efficiency<sup>[1]</sup>. For the control FETs, the power MOSFET must exhibit low gate charge and capacitance to

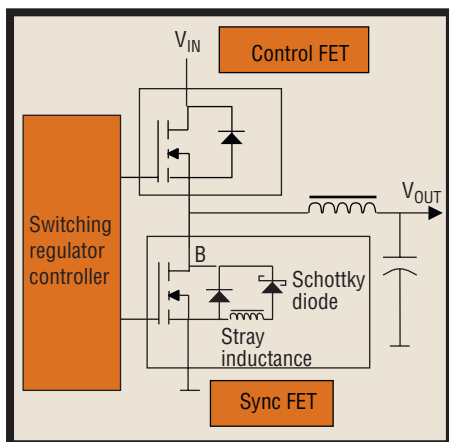


Fig. 1. Sync-buck dc-dc converter topology.

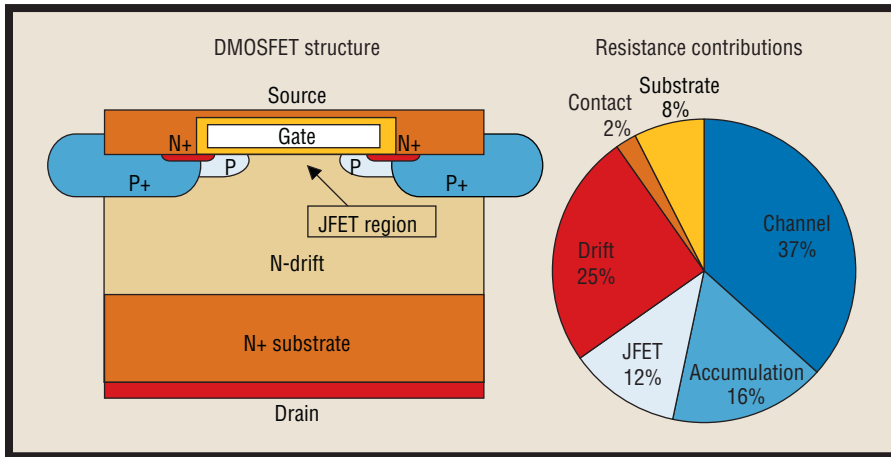


Fig. 2. DMOSFET structure and its internal resistance distribution.

reduce the switching losses while maintaining reasonably low on-resistances. A smaller input capacitance for a control FET enables fast turn-on and turn-off transients without requiring high drive currents from the controller. In the case of the sync FET, a low on-resistance is paramount because it operates at a high duty cycle. To pre-

vent inadvertent  $CdV/dt$  induced turn-on, which can lead to destructive shoot-through currents, these devices must have a small  $[C_{gd}/C_{gs}]$  ratio, where  $C_{gd}$  is the gate-to-drain capacitance (Miller capacitance) and  $C_{gs}$  is the gate to source capacitance (input capacitance).

The sync-buck circuit operation

also requires a short “dead time” between switching the top and bottom power MOSFETs because they would short-circuit the input power supply if turned on simultaneously. During this dead time, the main inductor current flows via the body diode of the sync FET. This leads to substantial power loss due to the relatively high-voltage drop across the P-N junction (when compared with the MOSFET voltage drop) and because of the reverse recovery loss associated with the stored charge.

A commonly proposed solution to reduce these losses and increase the efficiency is the addition of a Schottky diode across the sync FET (Fig. 1). Due to the short time duration of the dead time when the Schottky diode is conducting the inductor current, the common practice is to use a Schottky diode rated at one-quarter of the current flowing through the inductor. This may be acceptable from the point

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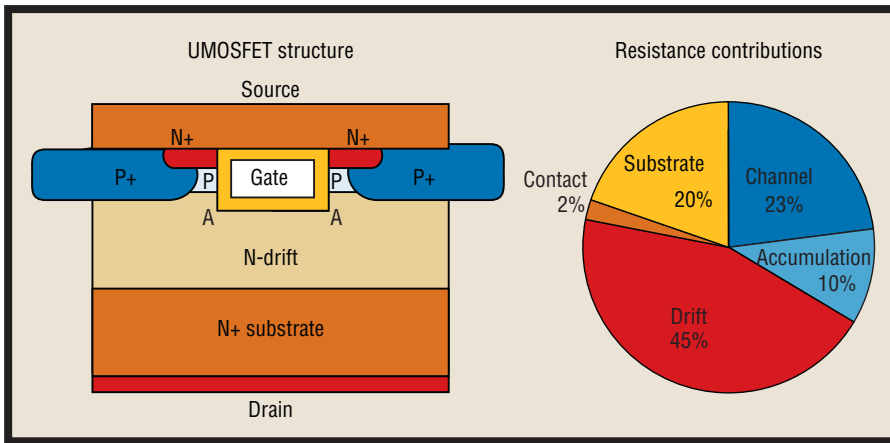


Fig. 3. Trench of UMOFET structure and its internal resistance distribution.

of view of the power dissipation in the Schottky diode as well as minimizing its leakage current.

However, the voltage drop across the Schottky diode when carrying the full inductor current can exceed the typical voltage drop in the body diode (0.7 V) of the sync FET, leading to the conduction of most of the inductor current through the body diode. Further, the stray inductance (Fig. 1) between the FET and the diode impedes the transfer of current from the MOSFET to the diode, defeating its utility. It has been suggested that the Schottky diode be co-packaged with the sync FET to overcome this problem, but the space occupied by the diode prevents the minimization of the on-resistance of the sync FET—leading to poor efficiency.

### Evolution of Power MOSFETs

Although the development of power MOSFETs began with the V-MOS structure, the first commercially successful devices were based on the DMOS structure<sup>[2]</sup>. In the DMOSFET structure (Fig. 2), the MOS channel is formed on the surface by the double-diffusion process with the channel length controlled by the relative diffusion depth of the P-base and N<sup>+</sup> source regions.

A more heavily doped P<sup>+</sup> region is added to the structure to suppress the turn-on of the parasitic npn transistor that is inherent in the MOSFET structure. Current flow from drain to source in the DMOSFET is induced

by the application of a gate bias to create a channel at the surface of the P-base region. The resistance in the path between the drain and source contains many components. The most important ones consist of the drift region, the JFET region, the accumulation region, and the channel region. In addition, for low-voltage (<30-V rated) devices, the contributions from the ohmic contacts and the N<sup>+</sup> substrate can't be neglected.

Analysis of the distribution of the resistances within the DMOSFET structure (Fig. 2) indicates that the channel contribution is dominant because of the relatively low channel density in the DMOSFET structure. The "Miller capacitance" in the DMOSFET can be reduced by decreasing the space between the P-base regions, but this is accompanied by an increase in the on-resistance<sup>[2]</sup>. The width of the gate must be optimized to achieve the best power MOSFET performance.

About five years ago, the power MOSFET industry shifted to a trench-gate technology to reduce the on-resistance. In the trench-gate structure (Fig. 3), commonly referred to as the UMOFET structure, the channel is formed on the vertical sidewalls of a trench etched into the silicon surface. Because the drain-source current is directed along a vertical path, the JFET resistance is eliminated. This allows reduction of the on-resistance not only by removal of one of the resistance components, but also by allow-

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ing a smaller cell size, which increases the channel density. Unfortunately, the trench-gate process is more complex and expensive when compared to the planar DMOS process.

The industry has also had to deal with reliability problems associated with high electric fields at the trench corners (labeled A in Fig. 3), which must be solved by rounding the trench corners and buffering the elec-

tric field using the P<sup>+</sup> regions. Further, the extension of the gate into the drift region increases the coupling between the drain and the gate leading to higher Miller capacitance and gate charge, which can adversely affect switching performance.

### Planar Architecture Revisited

Silicon Semiconductor Corp. has re-engineered the planar power

MOSFET structure to achieve performance metrics superior to those of state-of-art trench-gate devices. By retaining a planar architecture, the fabrication process remains compatible with mainstream CMOS process lines and reliability issues are ameliorated. In addition, this architecture has allowed implementation of a silicided gate stack to reduce the internal gate resistance of the MOSFET. The SSCFET structure (Fig. 4) contains a deep P<sup>+</sup> region that is self-aligned to the gate region<sup>[3]</sup>. Its higher doping concentration and deeper extension in both the vertical and lateral directions are used to create a potential barrier in the transition region, which is located below the gate region. The gate width and transition region doping profile are optimized to obtain enhanced power MOSFET performance. The screening of the gate region at B from the drain potential allows shortening of the channel length, without fear of reach-through-induced breakdown, to reduce its resistance contribution. The channel contribution (Fig. 4) decreases to half that observed in typical DMOSFETs, enabling specific on-resistances for SSCFETs to approach those obtained in typical trench MOSFETs.

The screening of the gate from the drain potential drastically reduces the Miller capacitance in the SSCFETs with typical values of C<sub>rss</sub> under 20 pF at a drain bias of 16 V<sup>[4]</sup> for a device with input capacitance C<sub>iss</sub> of 3000 pF. The ratio of [C<sub>rss</sub>/C<sub>iss</sub>] for the SSCFET is typically less than 0.01—an order of magnitude better than for typical trench MOSFETs. This provides power supply designers the opportunity to improve the efficiency of dc-dc converters by reducing the switching times without fear of CdV/dt-induced turn-on and shoot-through problems.

The screening of the gate region from the drain potential in the SSCFET allows a significant reduction of gate charge as well. The reduced gate drive currents for SSCFETs places a smaller burden on controllers, enabling migration to a higher operat-

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ing frequency. The SSCFETs exhibit remarkably low-gate reverse transfer charge ( $Q_{gd}$ ), which, in conjunction with the low internal gate resistance (under  $1 \Omega$ ), translates to short rise and fall times in applications<sup>[4]</sup>. The industry benchmark figure-of-merit product [ $R_{DS(on)} * Q_{GD}$ ] for the 30-V rated SSCFET is less than  $20 \text{ m}\Omega\text{-nC}$ , which is half that of typical trench MOSFETs. This is particularly significant for reducing the switching losses in the control FET leading to an increase in converter efficiency at operating frequencies from 200 kHz to more than 1 MHz.

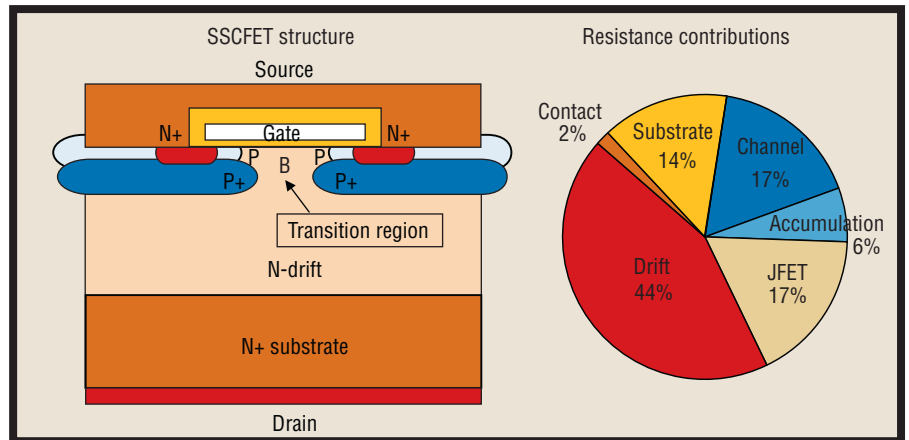


Fig. 4. SSCFET structure and its internal resistance distribution.

## JBSFET Technology

The sync-buck converter must be operated with sufficient dead-time between turning on and off the high-side and low-side power MOSFET to prevent a shoot-through problem. During the dead time, the inductor current flows via the body diode of the sync-FET unless an external Schottky diode is connected across it (Fig. 1). The transfer of current between the MOSFET and the Schottky diode is impeded by the presence of the stray inductance in the packages and the circuit board. One solution that has been

proposed is to co-package the Schottky diode with the power MOSFET. However, this takes up valuable space within the package, resulting in high on-resistances for the sync FET.

A new power MOSFET cell structure has been created, called JBSFET (Junction Barrier controlled Schottky Field Effect Transistor) that integrates the Schottky diode into the power MOSFET. In this structure, the Schottky diode is formed by making a break in the P-base and the P<sup>+</sup> shielding regions. The P<sup>+</sup> shielding region located below the

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Schottky contact produces a junction barrier at C (Fig. 5) that protects the Schottky contact from the drain potential. This design suppresses the well-known Schottky barrier-lowering phenomenon that leads to a rapid (typically 10 times) increase in leakage current with increasing reverse bias<sup>[2]</sup>. The junction barrier concept was first proposed and applied to improving the performance of Schottky rectifiers<sup>[5, 6]</sup>. In the JBSFET, the same P<sup>+</sup> shielding region used for achieving the channel length reduction in the MOSFET is simultaneously used to shield the Schottky contact with no additional process steps. Due to a high level of integration, the Schottky region has sufficient area to be able to handle the full current rating of the MOSFET.

At the same time, the leakage current in the JBSFET does not increase as rapidly with reverse voltage as in a typical Schottky rectifier<sup>[4]</sup>. The forward-voltage drop of the JBS (Junction-Barrier-controlled Schottky) diode in the JBSFET is less than 0.7 V at the maximum-rated current of the MOSFET. This suppresses the injection of minority carriers from the P-N body-diode of the MOSFET. Consequently, the JBSFETs exhibit lower power losses in dc-dc converters because the on-state voltage drop of the diode is smaller during the dead time, and no reverse recovery loss is associated with the stored charge in the body-diode of the MOSFET. Because the JBS diode is highly interdigitated with the MOSFET, no current transfer occurs even within the JBSFET chip, eliminating the problems that have been observed with external or co-packaged designs.

The JBSFETs offer on-resistances that are competitive with trench MOSFETs in equivalent packages while providing the added benefit of including the Schottky diode. This has been found to result in significantly higher efficiency (two to eight percentage points) in the dc-dc converter operating at 200 kHz to more than 1 MHz.

The planar power MOSFET structure has been re-engineered to enhance the on-resistance and gate charge by use of a deep P<sup>+</sup> region to shield the gate and channel regions. The resulting shortening of the gate width and the channel length has allowed dramatic improvement in the specific on-resistance and the  $[R_{DS(on)} * Q_{GD}]$  figure-of-merit. In addition, a power MOSFET die, with monolithically integrated Schottky diode that can handle the full current rating of the MOSFET, has been created by incorporating the Schottky contact within the power MOSFET cell structure. The same P<sup>+</sup> shielding region has been used to create

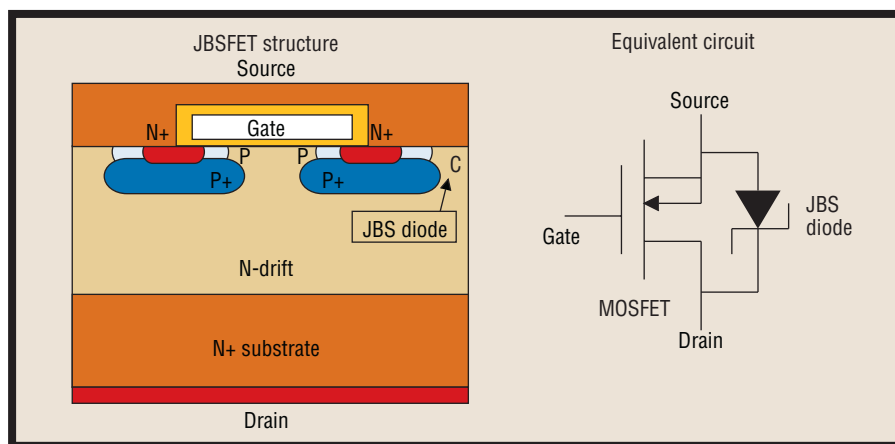


Fig. 5. JBSFET structure and its equivalent circuit with Junction Barrier controlled Schottky diode.

a JBS diode, which exhibits less increase in leakage current with reverse bias. The resulting SSCFETs and JBSFETs provide optimum power switches, as control FETs and sync FETs in dc-dc converters for high frequency (200 kHz to more than 1 MHz) voltage-regulator applications, to enhance the efficiency by 2% to 8%, while reducing the power device footprint by 200% to 300%. PETech

**Because the JBS diode is highly interdigitated with the MOSFET, no current transfer occurs even within the JBSFET chip, eliminating the problems that have been observed with external or co-packaged designs.**

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