Digitally Controlled Power Supply Design Wizard

by

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1 Abstract

Digitally controlled power supplies offer a myriad of programmable features to the system engineer such as control loop modifications, sequencing and tracking, interleaving, protection and monitoring features. Configuring such a power system is greatly eased by the use of such tools as the design wizard recently introduced as part of Power-One's PC-based GUI for use with the Z-One™ Digital IBA solution. The wizard takes only a few basic inputs such as voltages and currents and configures a complete system including part selections and settings. An auto-compensation feature is provided so that one can choose the output capacitors best suited for an application, then "build" the control loop around them instead of vice versa. Input and output ripple are reduced by automatic intelligent interleaving. After the wizard is completed, the system parameters can be manually edited if desired. The completed system can also be simulated within the GUI to see the predicted ripple and transient behavior.

2 Introduction

The Z-One™ Digital IBA is a complete, feature rich power system solution for the Intermediate Bus Architecture (IBA). Currently, members of the Z-One family include Point-Of-Load (POL) regulators, the Digital Power Manager (DPM), and the Graphical User Interface (GUI) for system configuration, simulation, and monitoring. A block diagram is shown in Figure 1. The GUI allows design and simulation of the system and outputs a configuration file for the DPM. The file is stored in the DPM's non-volatile memory. Upon power-up, the DPM initializes the POLs to the desired configuration.

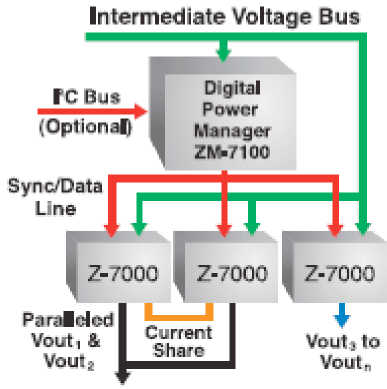

Figure 1. Z-One Block Diagram

2.1 Z-One Features

Due to space constraints, only some of the features will be covered here. Refer to the data sheets available at http://www.power-one.com/products/Z.html for more information.
The Z-One system uses a digital control methodology to provide a multitude of features and flexibility with a minimum number of parts. The data sheet of a typical Z-One POL lists the following features, where the highlighting indicates digitally configured features.

ZY7115 POL Features

- Wide input voltage range: 3V – 13.2V
- High continuous output current: 15A
- Active digital current share
- Single-wire serial communication bus for frequency synchronization, programming, and monitoring
- Wide programmable output voltage range: 0.5V to 5.5V
- Optimal voltage positioning with programmable slope of the VI line
- Overcurrent, overvoltage, undervoltage, and overtemperature protections with programmable thresholds and types
- Programmable fixed switching frequency 0.5-1.0MHz
- Programmable turn-on and turn-off delays
- Programmable turn-on and turn-off voltage slew rates with tracking protection
- Programmable feedback loop compensation
- Power Good signal with programmable limits
- Programmable fault management
- Start up into the load pre-biased up to 100%
- Full rated current sink
- Real time voltage, current, and temperature measurements, monitoring, and reporting

Likewise, the DPM has many programmable features of its own, and supports the POLs' programmable features as well by holding all the POL configuration data. Below is a list of the DPM feature with the highlighting indicating digitally configured features

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ZM7100 Series DPM Features
• Programs, controls, and manages up to 32 independent Z-series POL converters via the single line digital Z-OneTM Bus
• Programs output voltage, protections, optimal voltage positioning, turn-on and turn-off delays and slew rates, switching frequency, interleave (phase shift), and feedback loop compensation of the Z-series POL converters
• User friendly ZIOSTM GUI interface for programming, monitoring, and performance simulation
• Intermediate bus voltage monitoring and protection
• AC Fail input
• Up to four programmable interrupt inputs
• Ring buffer with programmable refresh rate to store real time voltage, current, and temperature measurements for up to 32 Z-POL converters
• Non-volatile memory to store system configuration information and status data
• 1 kbyte of user accessible non-volatile memory
• Control of industry standard DC-DC front ends
• Crowbar output to trigger the optional crowbar protection
• Four independent OK lines for flexible fault management and fast fault propagation

3 The Design Wizard

3.1 The Need For A Design Wizard

The Z-One system can operate with default parameters. However, the performance can be greatly enhanced by tailoring the configuration to the needs of the specific application. There is a logical way in which the detailed configuration can be flowed down from the system requirements, so most of the configuration details can be derived from the top-level requirements by software. The Design Wizard is a time saving feature of the GUI that does just that.

3.2 Design Wizard Features

The Design Wizard asks the user a few basic questions about the system requirements such as the intermediate bus voltage, number of outputs, and voltages and currents of each output. The Wizard then selects the best combination of POLs and DPM part numbers to minimize the parts count and system cost. The part selections can further be changed by the user to trade part count, part commonality, or to account for a user's preference toward a particular part (see Figure 2).

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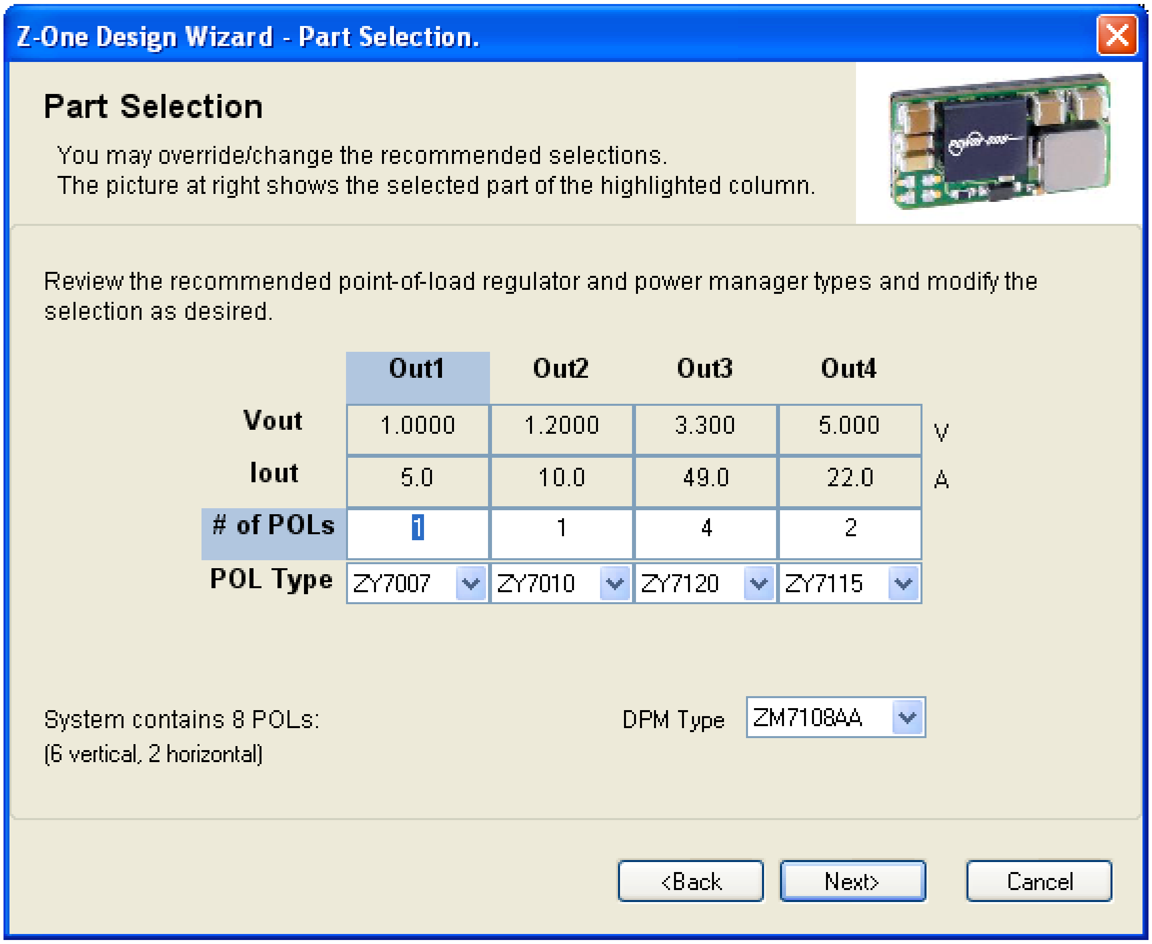

Figure 2. The part selection window.

POLs are then automatically assigned to a unique address within the system and are assigned to the appropriate output bus. The POLs are interleaved according to an algorithm that reduces both input and output ripple. The duty cycle and current limits are also calculated and set. The user specified margining is applied to all POLs. The sequencing, output over- and under-voltage limits, and power good threshold are set to default values. The loop compensation of each POL can be optimized based on the output capacitors used.

DPM - The input over- and under-voltage limits for the IBV are set according to the user's specified range. The entire system can be allowed to turn on as soon as power is applied or wait for a logic-level or I^2C command. Parametric and status monitoring are set to a 1 Hz update rate.

After running the Design Wizard, the System Configuration window is displayed as shown in Figure 3.

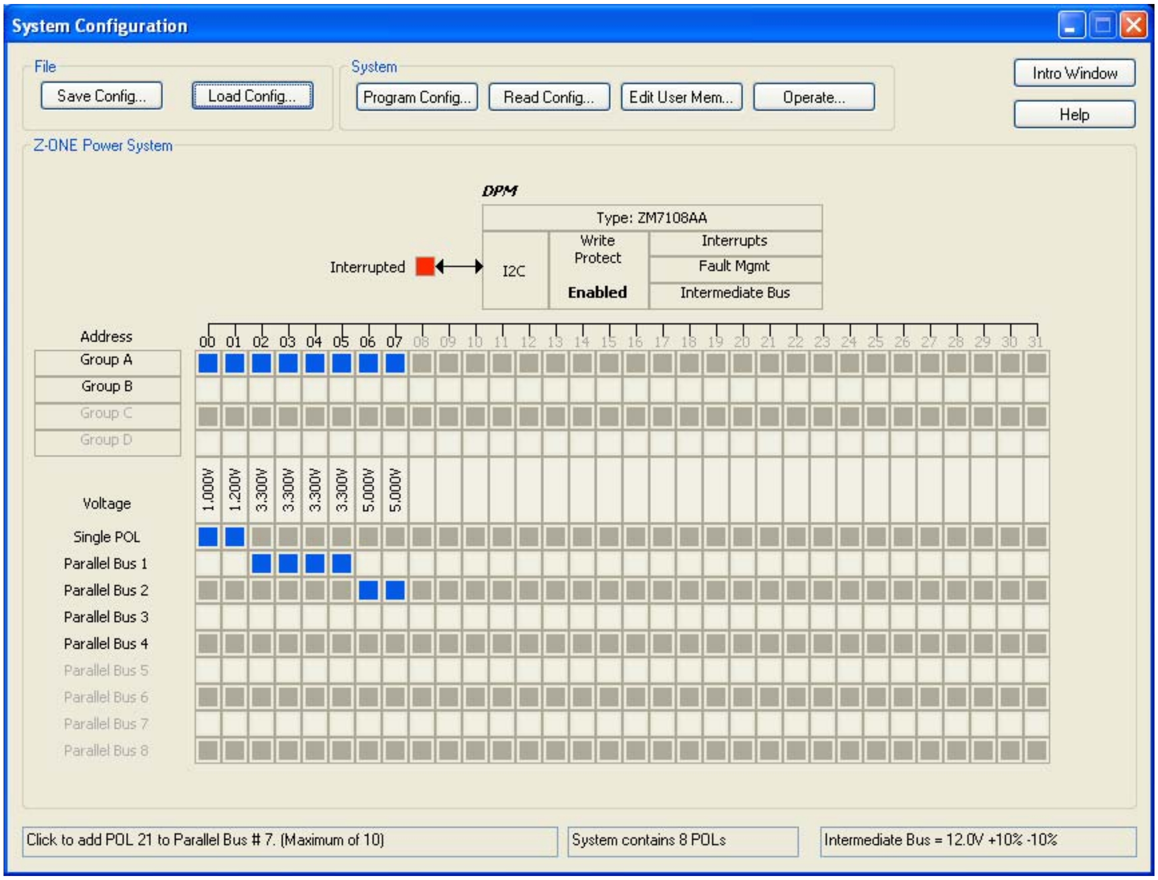

Figure 3. Typical results from Design Wizard.

3.3 Design Wizard Implementation

3.3.1 Input Over- and Under-Voltage Protection

The user is asked to supply the range of input voltages over which the system will operate. This can be input as a nominal value and tolerance, or minimum and maximum values. These values are used for the input over- and under-voltage protection settings – outside of which the system is shut down.

3.3.2 Vout Setup

The Vout settings are taken directly from user input. Load regulation is required to be set on all but one of a group of paralleled POLs so the wizard takes care of this. The wizard also prevents the user from selecting an output voltage that is too high for a given input voltage based on the maximum duty cycle consideration.

3.3.3 POL & DPM Selection

For each output, one or more POLs of the same type may be used as determined by the required output current. When POLs are paralleled, their current rating must be derated to 80% to account for mismatches in current sharing. The software calculates the number of each available POL type needed to meet the output current requirement and selects the

POL type that yields the minimum quantity of POLs. This also minimizes the cost. The POL selection algorithm is shown in Figure 4.

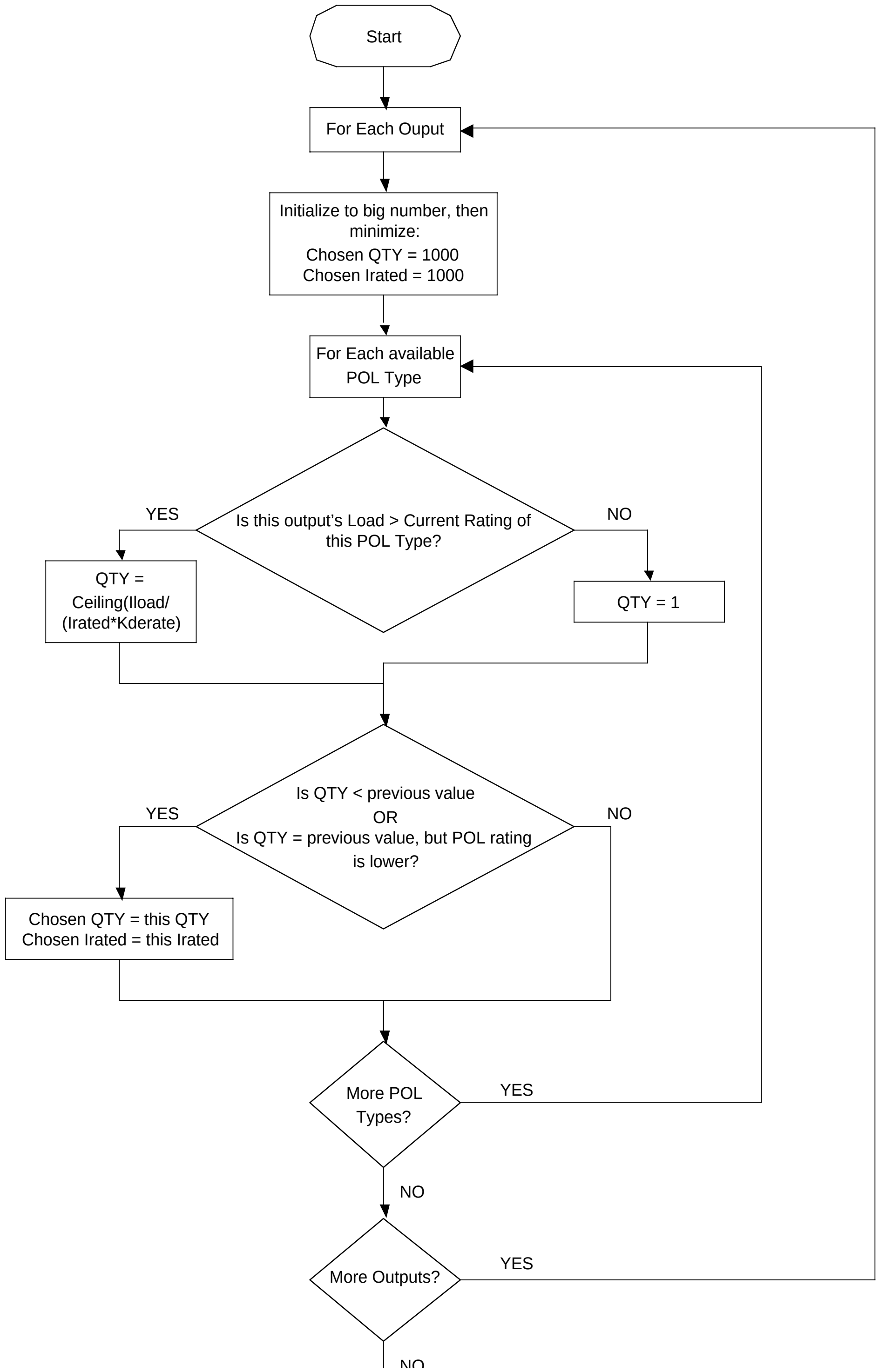

Figure 4. Algorithm for POL selection.

The various types of DPMs vary in the number of POLs and output buses they can handle. Once the POLs have been chosen for each output, the total number of POLs and parallel buses in the system is counted and the appropriate DPM is chosen.

3.3.4 Auto Interleaving

Interleaving – applying a phase shift between the switching actions of multiple converters operating at the same frequency – is an effective means of reducing both input and output switching ripple and spikes. Interleaving is applied so that the switching ripple tends to cancel. For parallel POLs, it is always optimal to have even spacing so their output ripple is minimized e.g.

Phase shift between parallel POLs = 360/(number of POLs in parallel) [degrees]

To minimize input ripple, the POLs connected to each output bus should have a phase offset as a group so they don't switch current to the input bus at the same time. The optimality condition for minimizing input ripple is not as straight-forward, but a simple group offsetting scheme that greatly reduces input ripple is as follows:

Offset angle between output buses = 360/(number of output buses) [degrees]

Also, a more complex scheme can be applied that takes into account the magnitudes of each load current. Input and output ripple are both minimized by applying the sum of the above two angles to each POL.

3.3.5 Auto Protections

The current limit of the POLs is chosen so that the minimum current limit threshold is above the specified bus current. All other protections are set to "Smart Default" values. Over- and Under Voltage, and Power Good are all functions of Vout and change as Vout is changed.

3.3.6 Duty Cycle Limit

The duty cycle limit for each POL is set to the maximum steady-state duty cycle plus headroom:

DCL = Min(1.95*Vout/Vin_min, 0.95)

3.3.7 The Control Loop

The feedback loop of the Z-One POLs is a fully programmable, digital Infinite Impulse Response (IIR) filter. The filter implements an integration pole, two lead compensation zeros, and two high frequency poles. The sample rate of the IIR filter is equal to the switching frequency which can be 500 or 1000 KHz. The z-domain transfer function of the error amp. IIR filter from the error signal to the duty cycle is:

$$\mathrm{Gea}(z) = \frac{\left(C0 + C1 \cdot z^{-1} + C2 \cdot z^{-2} + C3 \cdot z^{-3}\right)}{\left(8 - B1 \cdot z^{-1} - B2 \cdot z^{-2} - B3 \cdot z^{-3}\right)} \cdot \frac{1}{20.48}$$

where the B's and C's are the digital filter coefficients.

The GUI does all the work of making the use of the digital filter transparent to the user. It does this by applying the bilinear transform to allow the IIR to be programmed in terms of the desired pole-zero frequencies rather than the digital filter coefficients. Starting with the desired frequency-domain response, with poles p1, p2, p3, and zeros z1, and z2:

$$\mathrm{Gea}(f) = \frac{p1}{j \cdot f} \cdot \frac{(j \cdot f + z1) \cdot (j \cdot f + z2)}{(j \cdot f + p2) \cdot (j \cdot f + p3)} \cdot \frac{p2 \cdot p3}{z1 \cdot z2}$$

the substitution is made:

$$f = \frac{2}{T} \cdot \frac{z - 1}{z + 1} \cdot \frac{1}{2 \cdot \pi \cdot j}$$

(where T is the sample period)

A large polynomial in z is created, the coefficients of which are matched to the z-domain filter equation above to arrive at the digital filter coefficients.

3.3.7.1 Auto-Compensation

Each POL type has default coefficients that work with most any application, but since the filter is programmable, it can be optimized to each particular application. The optimization can be done manually by adjusting the pole-zero frequency scroll bars in the GUI, or automatically using the GUI's new auto-compensation feature.

With the programmable IIR, we have the ability to optimize the feedback compensation based on the actual output capacitance and input voltage. This is important since the loop gain, and therefore the transient performance and stability, are a function of these parameters.

Once the output capacitors and their ESR are specified, the coefficients of the IIR filter are optimized by performing repeated time-domain and AC simulations. After each simulation, certain performance criteria are evaluated and the partial derivatives of the performance criteria with respect to each filter parameter are computed.

These partial derivatives are used to update the filter parameters and the process is repeated until the design goals are met. Due to the nature of the digital filter, discontinuities can occur in the partial derivatives, making it difficult to determine how to update the filter parameters. In this case, a least squares estimation technique is used.

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The design goals include, minimizing the transient response in both amplitude and recovery time, having a phase margin of 45 degrees, and minimizing the noise bandwidth of the control loop.

By adjusting the control loop compensation (manually or using auto-compensation), the POL can work optimally with any type of output capacitor from low ESR tantalum to ceramic, to OSCON, or a combination of various kinds. The Auto-Compensation user interface is shown in Figure 5.

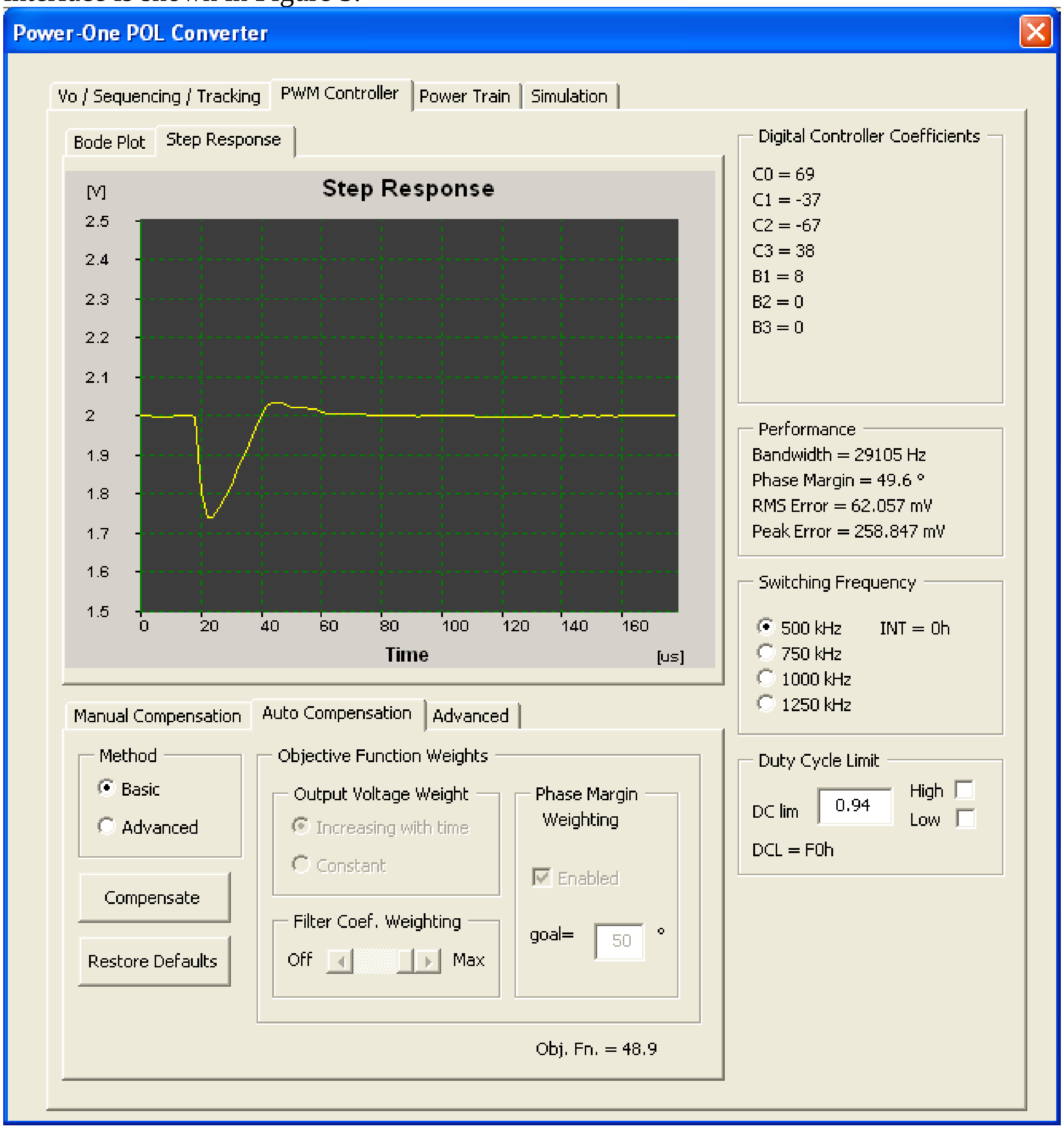

Figure 5. Auto-Compensation user interface.

4 Verification by Simulation

Once the configuration is completed, each POL can be simulated within the GUI in both time-domain and frequency-domain. In the time-domain, the turn-on sequencing and transient line and load responses and ripple can be seen as shown in Figure 6. If the control loop has been optimized, yet the transient response is still not acceptable, this indicates that more output capacitors (or capacitors with lower ESR) are required.

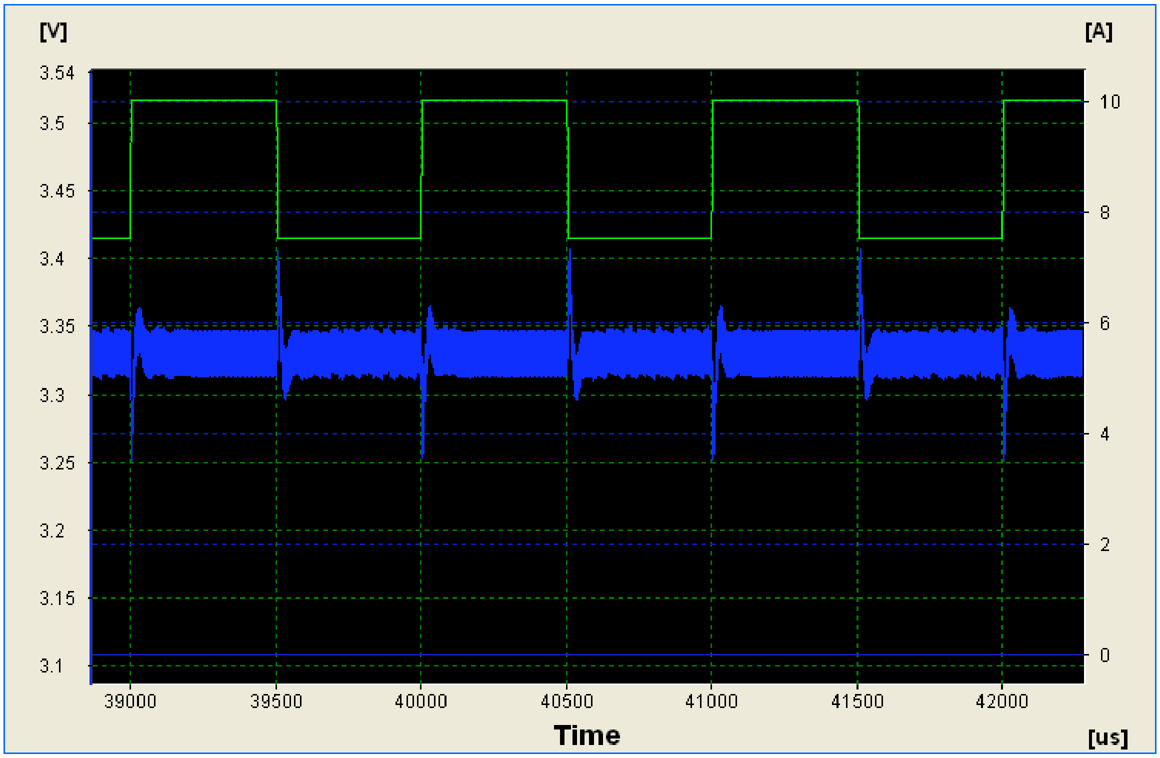

Figure 6. Typical time-domain simulation results with pulsed load.

In the frequency-domain, the loop's crossover frequency and phase margin can be seen. The conservative range for cross-over frequency is 10 to 20 KHz, however it can be as high as about 1/10 the switching frequency. The phase margin is recommended to be above 45 degrees; otherwise the system will ring excessively or oscillate. Using the auto-compensation tool will make sure that these goals are met.

5 Summary and Conclusions

The Design Wizard significantly streamlines the process of configuring a Z-One power system by translating the top-level requirements into a valid configuration file within about 10 minutes for a typical 4-output system. The configuration can be further customized and simulated as desired. Any changes can be handled without having to replace or add external components – even during integration and test of the target system.