COMPENSATING DIGITAL PWM CONTROL LOOPS

By

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Abstract: Digital pulse width modulators (PWM) are emerging in commercially viable power supply control ICs. Although digital PWMs provide many benefits in terms of flexibility and power system management, they also present some challenges to power supply designers not familiar with digital signal processing (DSP) techniques. This difficulty is evident when compensating the power supply control loop. This paper will show the parallels between the analog control loop and the digital control loop. It will be shown that each block in a digital control loop can be represented by a continuous "s" domain transfer function, and thus can be modeled or simulated with commonly available programs such as MathCAD. Using a minimum of DSP theory, equations are derived which allow the designer to calculate digital filter settings (coefficients) with a calculator. The paper will show a worked example with test results from a power supply controlled by a digital PWM.

Introduction: The use of digital techniques to control power supplies promises many advantages over the use of discrete components. Like its analog counterpart, a digital control loop has a reference to set the output voltage, an error generating mechanism, an integrator to minimize error, and a compensation filter to provide loop stability. In an analog controller, the reference is provided with a trimmed band-gap device. The error generator, integrator, and compensating filter are combined in an op-amp circuit often referred to as a type 3 amplifier. In both the analog and digital control loops the errors due to the reference can be reduced with trimming. The errors in the analog compensating filter can be calculated with classical circuit analysis techniques and quantized as gain and phase values versus frequency. The digital control loop generates an error signal by first digitizing the power supply output voltage, and then subtracting the reference value from the digitized output voltage value. The integration function is accomplished with an accumulator. Like an analog integrator, small errors over a period of time will increase to provide an output that will act to reduce the output error. The digital implementation of the compensation filter deviates significantly from its analog dual. The digital compensator is realized with a cascade arrangement of multipliers and storage registers. This method of digital compensation is often referred to as a recursive filter, and the factors A, B and C in the multipliers are called coefficients. By selecting values for the coefficients the gain, Q and zero frequencies can be set. By using the pole-zero matching technique, a set of equations are obtained that map the frequency domain requirements for gain, Q, and zero frequencies to multiplier coefficients. Once the coefficients are selected, the recursive filter's performance can be calculated. The filter can also be modeled and simulated in the frequency domain both independently and as part of the entire power supply control loop. Simulation results can easily be compared to test results from the actual circuit implementation.

II. Buck Power Converter Model and Compensation Requirements

The power stage model is common to both analog controlled and digitally controlled power supplies. A popular topology, and the topology used as an example in this paper, is the synchronous buck converter. A simplified schematic of this converter is shown in Figure 1.

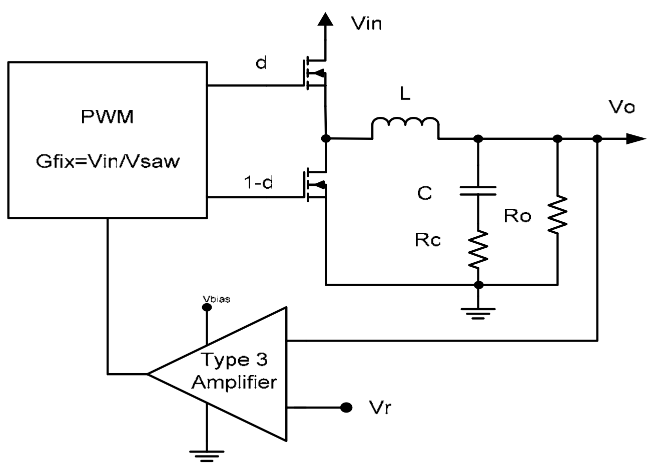

Figure 1 Simplified Synchronous Buck Converter

The small signal transfer function of this converter in voltage control mode is well known (1) and is described by the following equation:

$$G = \frac{G_{fix}}{1 + 2\delta s / w_n + s^2 / w^2{}_n}$$

This equation describes the transfer function from the input to the PWM to the output voltage, Vout, called the control to output transfer function. The Bode plot of the control to output transfer function is shown in Figure 2. This transfer function is shared by the analog controlled and digitally controlled converters.

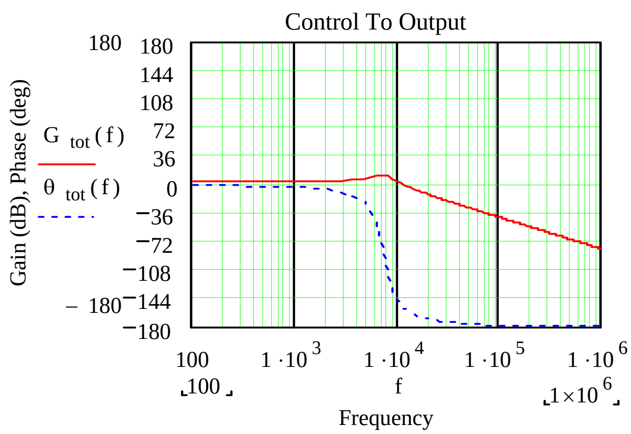

Figure 2 Buck Converter Control to Output Bode Plot

The control to output transfer function is comprised of 2 parts; the LC filter and the fixed modulator gain G_{fix}. The characteristics of the LC filter are analyzed in detail in (1) and (4) with the results summarized here. The LC filter has -180 degrees of phase shift and has an attenuation of 40 dB per decade above its natural frequency f_n. The resonant frequency of the LC filter is calculated by using the equation below:

$$f_n := \frac{\frac{1}{\sqrt{L \cdot C}} \cdot \sqrt{\frac{Rmax + Rs}{Rmax + Rc}}}{2 \cdot \pi}$$

Where Rmax is the highest expected output resistance, Rc is the capacitor Equivalent Series Resistance (ESR), and Rs is the combination of the inductor ESR and MOSFET on resistance. LC filters exhibit resonant behavior. Near the natural frequency f_n the LC filter transfer function will effectively amplify the input signal and exhibit a rapid phase shift from 0 to -180 degrees. The extent to which this occurs is determined by the Quality factor (Q). The Q of the LC filter is calculated using:

$$Q := \frac{\frac{1}{2 \cdot \pi \cdot f_n}}{C \cdot Rc + \frac{(C \cdot Rmax \cdot Rs) + L}{Rmax + Rs}}$$

The fixed gain in an analog PWM is a constant and has virtually no phase impact to the feedback loop. The DC gain of the transfer function is defined by

$$G_{fix} = Vin / Vsaw$$

Where Vin is the power supply input voltage and Vsaw is the peak to peak magnitude of the PWM saw-tooth signal. The goal of the compensation circuit is to modify the gain and add phase to the frequency response of the modulator and LC filter stage of the power supply to achieve the desired feedback gain and phase shown in Figure 3.

Comparing Figures 2 and 3 reveals what the frequency response of the compensation circuit should be. This is shown in Figure 4.

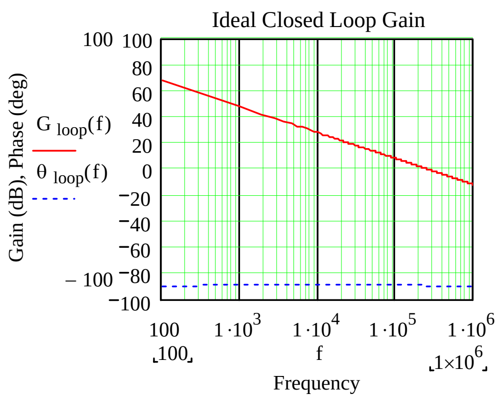

Figure 3 Desired Closed Loop Bode Plot.

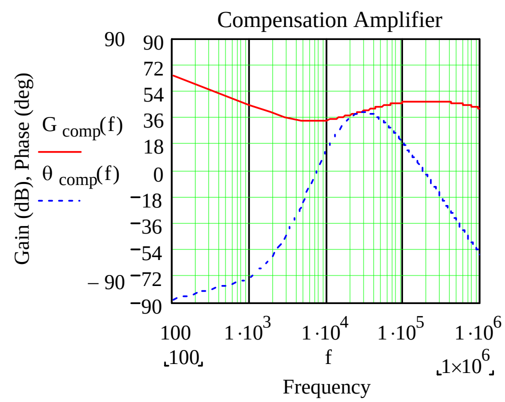

Figure 4 Type 3 Amplifier Bode Plot.

In a voltage mode analog power supply this compensation is done with resistors and capacitors configured to provide poles, zeroes and gain in the error amplifier. A common compensation amplifier is shown in Figure 5, and is referred to as a type 3 compensation amplifier (4). The type 3 amplifier combines the summing junction, integration and compensation functions.

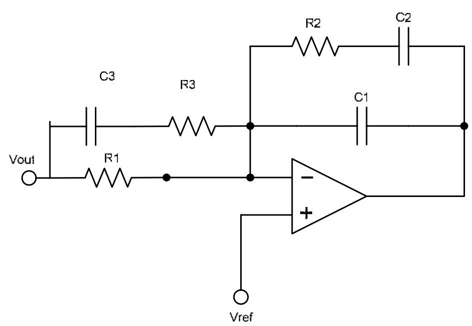

Figure 5 Type 3 Compensation Amplifier

The following equations are used to calculate the component values needed in the compensation amplifier.

$$R2/R1 = G_{comp} \quad C2 = 1/2\pi f_{z1}R2 \quad C1 = 1/2\pi f_{p1}R2 \quad C3 = 1/2\pi f_{z2}R1 \quad R3 = 1/2\pi f_{p2}R1$$

Where G_{comp} is the desired DC gain, f_{p1} and f_{p2} are pole frequencies and f_{z1} and f_{z2} are zero frequencies. The method for selecting the gain and frequencies for the compensation amplifier is explained in detail in (4). First, a crossover frequency f_{xo} is selected to be some fraction of the power supply switching frequency. The example circuit in this paper uses $f_{xo} = f_s/40$, however a much higher frequency could be used.

Next the DC gain needed for this compensator is calculated by assuming a -1 gain slope for the compensated control loop for a given crossover frequency expressed as

$$G_{comp} = f_{xo} / f_s G_{fix}$$

The 2 zeroes are selected to be less than the lowest expected f_n, in order to have sufficient phase margin. Lastly, the compensator provides 2 additional poles to keep the error amplifier from operating beyond its gain-bandwidth product limit and keep switching frequency ripple from interfering with the operation of the PWM circuitry.

III. The Digital PWM

The digitally controlled power supply block diagram can be shown to differ from the analog version only by the values assigned to the PWM block and the compensation block. The gain of the digital PWM block is unique to individual digital architectures. In general, a digital controller has an A/D converter, a summing register, a compensation filter, an accumulator, an anti-aliasing filter, and a digital PWM. Although the methods of modeling A/Ds, accumulators and DPWMs is beyond the scope of this paper, the A/D converter, summing register, and digital PWM can be modeled with constants and delays, as long as they are operated at frequencies much higher than the frequencies of interest in the control loop. The example circuit block diagram is shown in Figure 6.

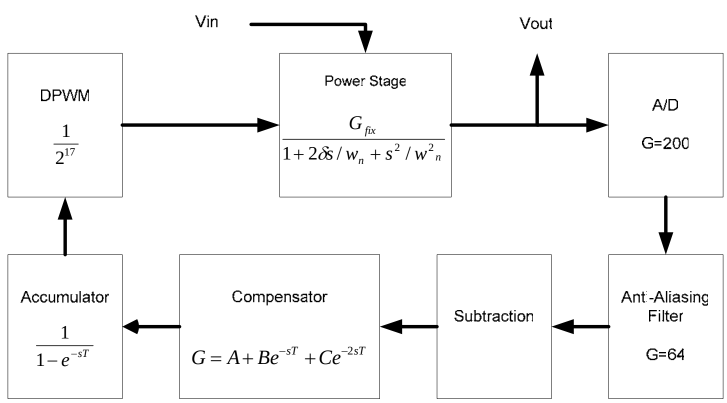

Figure 6 Digital Control Block Diagram

In this circuit the error signal is applied to the A/D converter, which converts this error voltage into a digital value. Its gain is 1/Vstep (1/5mV) or 200. Following the A/D converter is the error generator. The error generator is simply a subtraction function which outputs a number that represents the output voltage deviation from the desired output voltage; in other words a numeric error signal. The error signal is passed through an anti-aliasing filter. The anti-aliasing filter is a multi-stage digital filter that provides signal gain and high frequency noise rejection. Its purpose is to attenuate any signals with frequencies above the Nyquist frequency, in this case $f_s / 2$. It has the added benefit of eliminating the need for the poles used in the analog compensator. The anti-aliasing filter has very high attenuation at the switching frequency without adding excessive phase loss. The anti-aliasing filter used as an example in this paper has a constant gain factor of

2^6 over the frequency range of interest, and its phase loss can be expressed as a function related to the switching frequency as given in

$$G_{alias} = 2^6 / e^{-sT}$$

Where T is the sample period, in this case is $T = 1/f_s$. Temporarily skipping the compensator, the output of the compensator is fed into the accumulator. In an analog compensator the high DC gain is provided by an integrator which is "built in" to the op-amp compensation circuit. In a digital implementation the integration is provided by an accumulator which has a gain of:

$$G_{acc} := \frac{f_S}{2\pi \cdot f}$$

The output signal from the accumulator is applied to the Digital Pulse Width Modulator (DPWM). The DPWM converts the compensator into the duty cycle which is applied to the power supply MOSFETs. The DPWM used in this example circuit has a gain of $1/2^{17}$. In order to mathematically map a direct correlation from the digital control loop to the analog control loop, the gain of the A/D, DPWM and decimation filter can be combined and represented in the PWM block of the simplified block diagram in Figure 1. In the same fashion, the adder, accumulator and compensator can be combined to provide the same functionality as a type 3 compensation amplifier also shown in Figure 1. In summary, the simplified digital control loop block diagram is drawn in Figure 8, and the control to output transfer function is given by:

$$G = \frac{G_{fix}}{1 + 2\delta s / w_n + s^2 / w^2{}_n}$$

Where $G_{fix} = 200 * Vin / 2^{11}$. Note the similarity between the analog and digital representations.

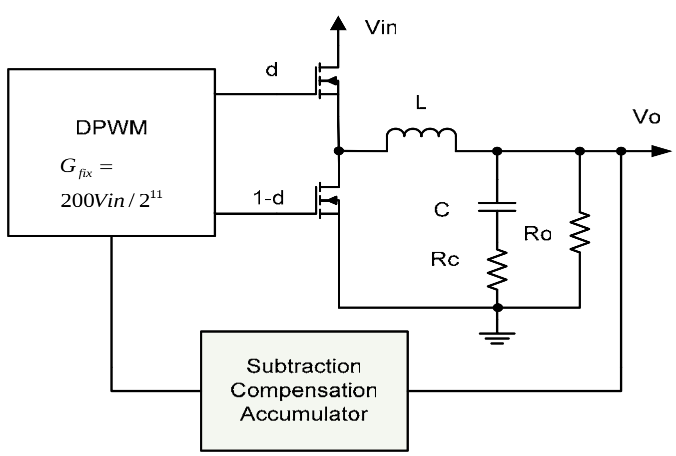

Figure 8 Simplified Digital Control Block Diagram

IV. Calculating Compensator Constants

The digital control loop is compensated in much the same way as the analog control loop. A crossover frequency is selected and the DC gain of the compensator is calculated, using a slightly different equation due the accumulator is used in the digital implementation:

$$G_{comp} := \frac{2\pi}{\left(\frac{f_s}{f_{xo}}\right)} \cdot \frac{1}{G_{fix}}$$

Like the compensator implemented with an analog op-amp, the digital compensator has 2 zeroes at the LC resonant frequency f_n. Instead of an op-amp circuit the digital compensator utilizes a recursive filter. A recursive filter is simply an adder with 3 inputs: the output of the A/D converter (the error voltage) multiplied by a constant, the error voltage from the previous switching cycle (shown as z^{-1}) multiplied by another constant, and the error voltage from the switching cycle 2 cycles previous (shown as an additional z^{-1}) multiplied by a third constant. This filter is shown schematically in Figure 9.

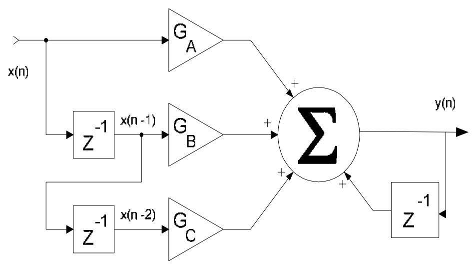

Figure 9 Recursive Filter

This recursive filter transfer function is

$$G_{comp} = A + Be^{-sT} + Ce^{-2sT} / e^{-sT}(1 - e^{-sT})$$

The term $1/1 - e^{-sT}$ is due to the accumulator shown as the z^{-1} block at the output of the summer in Figure 9, and models both the gain and phase response of the accumulator stage. The $1/e^{-sT}$ term represents the combined phase lag due to the delays inherent in the anti-aliasing filter, A/D, and accumulator. Although in a transcendental form, the filter described by this equation can be configured to have the same response as the analog filter by selecting appropriate constants for A, B, and C listed above. This can be done utilizing the following equations, derived using the pole-zero matching technique detailed in (2) and (3):

$$R := e^{\frac{-\pi}{Q\cdot\frac{f_s}{f_n}}} \qquad A := \frac{G_{comp}}{1 - 2\cdot R\cdot\cos\left(\frac{2\pi\cdot\sqrt{1-\frac{1}{4\cdot Q^2}}}{\frac{f_s}{f_n}}\right) + R^2}$$

$$C := A\cdot R^2 \qquad B := -A\cdot 2\cdot R\cdot\cos\left(\frac{2\cdot\pi\cdot\sqrt{1-\frac{1}{4\cdot Q^2}}}{\frac{f_s}{f_n}}\right)$$

As in the analog compensator case before, select the zero frequencies and gain desired for the compensator stage. Note that the digital compensator also provides a means of correcting for the Q of the LC filter. By using the equations above both the gain and phase of the LC filter will be cancelled by digital compensator, as shown in Figure 10. Since the digital control loop has an anti-aliasing filter that provides attenuation sufficient to guarantee noise immunity above fs/10, poles are not needed in the digital compensation filter. The closed-loop power supply can now be simulated and tested in the same manner as an analog controller.

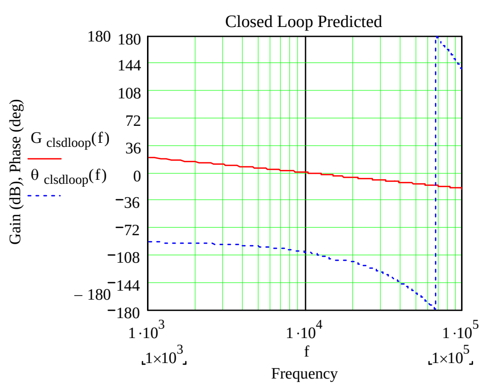

Figure 10 Digital Closed Loop Bode Plot

V. Design Example Analysis and Verification

The circuit in Figure 11 was used to illustrate the process of compensating a digital control loop. The component values are as follows: Vin=5V, Rmax=1MΩ, Rs=12mΩ, Rc=1mΩ, C=188uF, L=0.56uH, $f_s = 400kHz$, $f_{xo} = f_s / 40$, Vo=1.5V

This results in the following values: f_n = 15.5kHz, Q = 4.2, G_{comp} = 0.322

Using the pole-zero matched equations yields: A = 5.605, B = -10.573, C = 5.289

These values were simulated using MathCAD and loaded into the digital compensator. The predicted and measured frequency responses are shown in Figures 11 and 12 respectively.

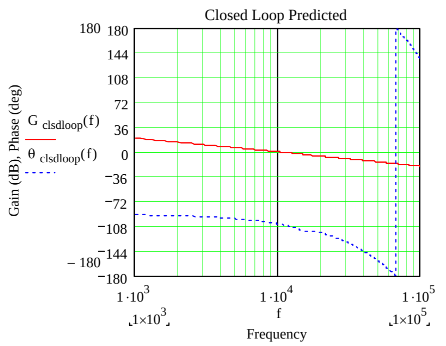

Figure 11 Predicted Bode Plot

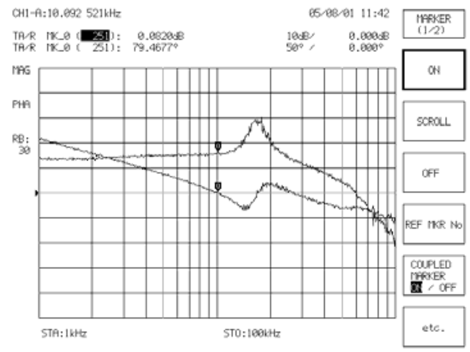

Figure 12 Measured Bode Plot

Note from the measured data that f_n is higher than expected, and the Q factor is lower than expected. This is due to using the zero DC bias and 100mV excitation rating for the capacitors, and using only device resistances for Rs, neglecting other parasitic circuit resistances. The component values were modified to reflect the operational values: Vin=5V, Rmax=1MΩ, Rs=20mΩ, Rc=1mΩ, C=103uF, L=0.56uH, $f_s = 400kHz$, $f_{xo} = f_s / 40$, Vo=1.5V

This results in the following values: f_n = 20.9kHz, Q = 3.5, G_{comp} = 0.322

Using the pole-zero matched equations yields: A = 3.151, B = -5.697, C = 2.869

Once again, these values were simulated using MathCAD and loaded into the digital compensator. The predicted and measured frequency responses are shown in figures 13 and 14 respectively. Now the predicted and measured response show the desired single pole roll-off and Q compensation desired.

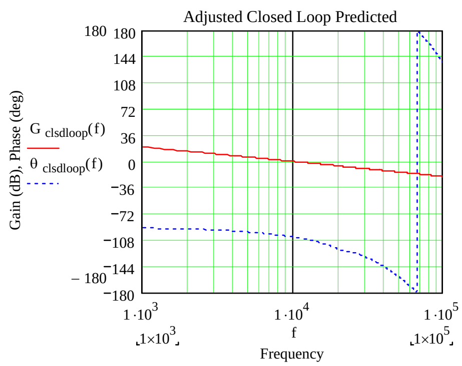

Figure 13 Adjusted Predicted Bode Plot

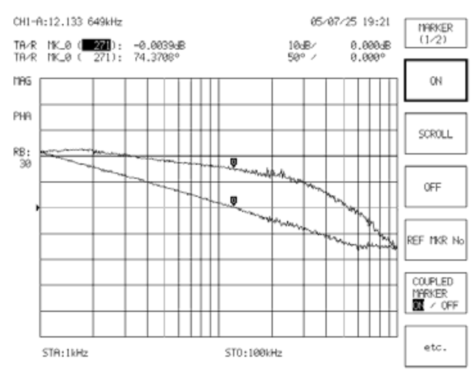

Figure14 Adjusted Measured Bode Plot

VI. Summary

By drawing parallels between traditional analog power supply control loops and a digital power supply control loop and mathematically combining the digital control functions in a convenient way, a direct mapping is made from the digital control loop to an analog one. By using pole-zero matched equations, and understanding the characteristics of the anti-aliasing filter used in most digital power supply controllers, the design of the compensator follows the same process as designing analog type 3 compensation amplifiers. Using these equations the performance of the digitally controlled power supply can be predicted, and the predicted performance closely correlates to measured results.

References

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