

# **An innovative Digital Controller for VRM Application with negligible quantization effects**

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## **ABSTRACT**

A mixed synchronous/asynchronous digital controller for high performance DC-DC converters is presented. The control architecture is quite simple, being based on the use of two digital-to-analog (DAC) converters with low resolution (7 bits). A new control algorithm exploits digitally generated current and voltage ramps in order to completely suppress quantization effects, despite the low resolution of the DACs. This algorithm, combined with the mixed synchronous/asynchronous control logic, makes the converter to behave in an analog-like fashion.

The digital controller has been implemented into a small, commercially available FPGA device and tested on a prototype single-phase buck converter operating at the switching frequency of 500 kHz. Output voltage tolerance within  $\pm 0.5\%$ , along with complete absence of quantization effects and fast transient response are experimentally demonstrated. The control architecture can be easily extended to multiphase converters. The features and the performance of the proposed architecture make it a valuable alternative for the control of DC/DC converters with tight voltage tolerance. Based on this new architecture, it has been designed a monolithic VRM controller by using the BCD VI (Bipolar, CMOS, DMOS) technology available from ST-Microelectronics. The controller is able to drive up to six phases and it is fully compliant with VRM10/11 Intel specifications.

## I. INTRODUCTION

Control of switchmode power supplies has been traditionally implemented using analog components for their low cost, high bandwidth, and proven technology. In recent years, there has been a growing interest in the implementation of digital control concepts in high frequency, low-to-medium power DC-DC converters. Digital control is well recognized for its flexibility and programmability, reduced design time, less susceptibility to aging and better noise immunity, ability to handle complex control schemes and to implement communication functions for fault and status information, easy reconfigurability for different applications [1-5]. Most of the digital controllers proposed so far are derived from the traditional voltage-mode analog controller [5]. An Analog-to-Digital Converter (ADC) is used to digitize the output voltage; a discrete-time control law calculates the duty-cycle and a Digital Pulse Width Modulator (DPWM) generates fixed-frequency signals for the power switches. The quantization arising from the finite word length of both ADC and DPWM produces undesirable effects on the output voltage, such as steady state errors and limit-cycle oscillations [6]. A longer word length would give better accuracy, but at the expense of a higher cost and complexity of the controller. For this reason, the current trend toward lower supply voltages and tighter voltage regulation is pushing the need for new digital control architectures that allow for reduced system complexity, while keeping high performance.

We have recently proposed a low-complexity digital control architecture, which employs only two Digital-to-Analog Converters (DACs) with low resolution (7 bits) [7-9]. The control architecture is based on a combination of current programming and variable frequency operation, and it exploits an original control algorithm to reduce quantization effects.

In this paper, we present an improved digital control algorithm capable of completely suppressing quantization effects, despite the use of low resolution DACs.

The key feature of the new control algorithm is the generation of a digital current ramp. This feature, combined with mixed synchronous/asynchronous control logic, makes the converter to behave in an analog-like fashion.

The paper is organized as follows: in Section II, we describe the new architecture and the control algorithm with reference to steady state and dynamic operation. The key features of the controller are highlighted and the design criteria are discussed. Experimental results are reported in Section III. Based on this new architecture, it has been designed a monolithic VRM controller by using the BCD VI (Bipolar, CMOS, DMOS) technology available from ST-Microelectronics. The controller is able to drive up to six phases and it is fully compliant with VRM10/11 Intel specifications. The integration is described in Section IV.

**II. DIGITAL CONTROL ARCHITECTURE**

A simplified block diagram of the digital controller applied to a single-phase buck converter is shown in Fig.1.

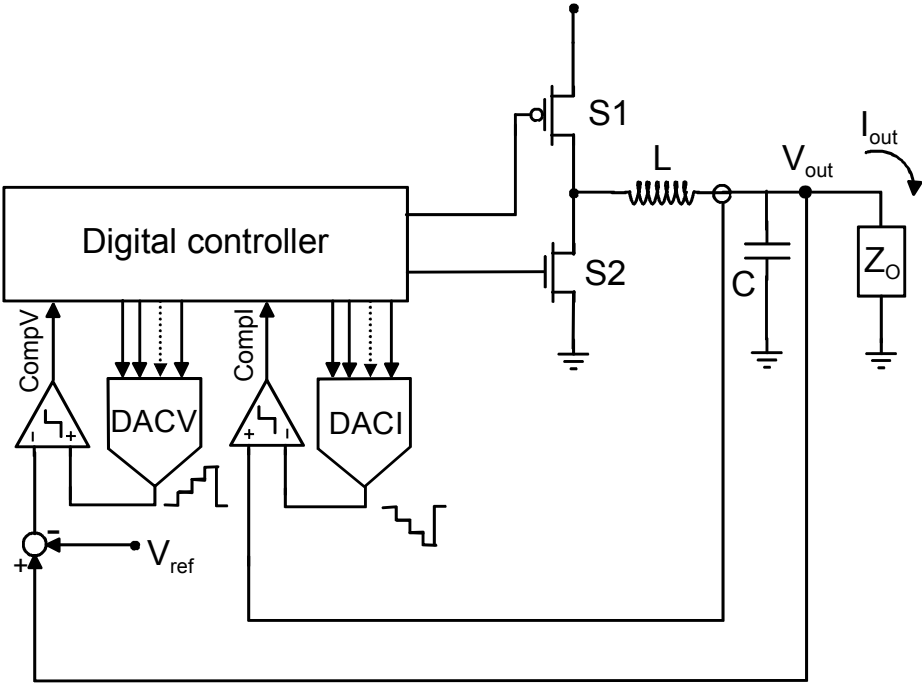


Fig.1 Simplified block diagram of the control architecture applied to a single-phase buck converter.

The error voltage,  $V_{err}=(V_{out} - V_{ref})$ , is compared to the reference signal generated by a first DAC (DACV). DACV generates a bottom voltage level,  $V_{low}$ , on which a voltage ramp with positive slope,  $SlopeV$ , is superimposed. The voltage ramp is generated digitally by incrementing the DACV input code at the clock frequency,  $f_{ck}$ . As soon as the DACV output voltage exceeds  $V_{err}$ , the voltage ramp is reset. The inductor current is sensed and compared to a current reference signal generated by a second DAC (DACI). DACI generates a peak current level,  $I_{pk}$ , on which a current ramp with negative slope,  $-SlopeI$ , is superimposed. Similarly to DACV, the current ramp is generated digitally by decrementing the DACI input code at the clock frequency  $f_{ck}$ . The current ramp is reset as soon as the inductor current exceeds the DACI reference signal.

Based on the status of the logic signals CompI and CompV, generated by the comparators, the digital core provides suitable control signals to the switches S1 and S2. The control laws can be summarized as follows:

- when the inductor current exceeds the reference signal generated by DACI (i.e., CompI="1"), switch S1 is opened and switch S2 is closed (PWM=OFF);
- when the reference signal generated by DACV exceeds the error voltage  $V_{err}$  (i.e., CompV="1"), switch S1 is closed and switch S2 is opened (PWM=ON).

It must be pointed out that the PWM signal is driven *asynchronously*, i.e., transitions are initiated by events (change of the status of CompI and CompV), and not by the system clock. Conversely, the beginning and the end of the digital ramps are *synchronous* with the system clock. This mixed synchronous/asynchronous control logic is a key feature of the controller, which is exploited for completely suppressing quantization effects.

### A. Steady state operation

The main signals of the controller operating at constant load current are shown in Fig. 2. Fig. 2a shows the inductor current  $I_L$ , the average inductor current  $\langle I_L \rangle$ , and the reference current generated by DACI, as a function of time. Fig. 2b shows the error voltage  $V_{err}$  and the voltage signal generated by DACV. The DAC outputs are slightly filtered, such that each step of the digital ramps has an exponential shape. For the sake of simplicity, the digital ramps will be considered linear: the effect due to their real shape will be considered later.

The steady-state average inductor current  $\langle I_L \rangle$  and output voltage  $V_{out}$  are given by:

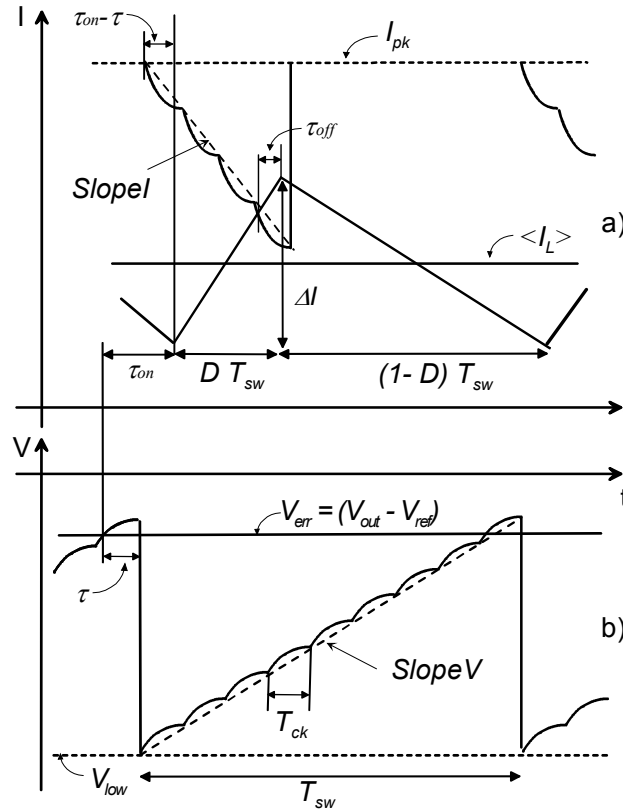


Fig.2 Current (a) and voltage (b) waveforms in steady state operation.

$$\langle I_L \rangle = I_{out} = I_{pk} - \frac{V_{out}(1-D)}{2L} T_{sw} + \tau_{off} \frac{V_{out}(1-D)}{LD} - Slope I (D \cdot T_{sw} - \tau_{off} + \tau_{on} - \tau) \quad (1)$$

and,

$$V_{out} = V_{ref} + V_{err} = V_{ref} + V_{low} + Slope V (T_{sw} - \tau) \quad (2)$$

where  $D$  is the converter duty cycle,  $T_{sw}$  is the converter switching period,  $\tau_{on}$  and  $\tau_{off}$  are, respectively, the turn-on and turn-off delays of the high-side switch S1, and  $\tau$  is the delay between the asynchronous switch-on command to S1 and the synchronous reset of the voltage ramp. It is worth noting that the switching period is discrete, being an integer multiple of the clock period,  $T_{ck}$ . In the implemented converter, the ramps are generated by increasing/decreasing the DAC input by one Least Significant Bit (LSB) each clock period. Therefore,  $SlopeI=LSB_{DACI}/T_{ck}$  and  $SlopeV=LSB_{DACV}/T_{ck}$ .

### B. Dynamic operation

As the load current exceeds the average inductor current, the error voltage lowers. This makes the average inductor current to increase due to the increase of the delay  $\tau$  and the reduction of the switching period. We investigate these two mechanisms separately, by first assuming  $|\Delta V_{err}| < LSB_{DACV}$ . In this case, the switching period of the converter and the current ripple amplitude do not change. However (see equation 1), the variation of the delay  $\tau$  makes the average inductor current to increase, until it balances exactly the load current. By looking at Fig. 2a, it can be easily realized that when  $\tau$  increases, the inductor current waveform shifts upwards rigidly. If  $\Delta\tau=T_{ck}$ , the average inductor current increases by  $SlopeI \cdot T_{ck}=LSB_{DACI}$ . Therefore, a continuous interval of average inductor current  $\Delta\langle I_L \rangle = LSB_{DACI}$  can be provided at a fixed switching period, due to the variation of the delay  $\tau$ . This result is independent of the actual shape of the current ramp.

If the load current increase is such that  $|\Delta V_{err}| > LSB_{DACV}$ , the switching period drops to the next available discrete value (Fig. 3). In order to evaluate separately the effect due to the reduction of the switching period, we assume that the delay  $\tau$  does not change. In this case, the increase of the average inductor current is given by:

$$\langle I_L \rangle_{n-1} - \langle I_L \rangle_n = \frac{V_{out}(1-D)}{2L} T_{ck} + SlopeI \cdot (D \cdot T_{ck}) \quad (3)$$

Note that the variation of the switching period makes  $\langle I_L \rangle$  to vary discretely.

By combining the two mechanisms described above, it turns out that a continuous interval of currents  $\Delta \langle I_L \rangle = LSB_{DACI}$  (arising from the variation of the delay  $\tau$ ) is associated to each discrete current level  $\langle I_L \rangle_n$  (due to the discrete variation of the switching period). As

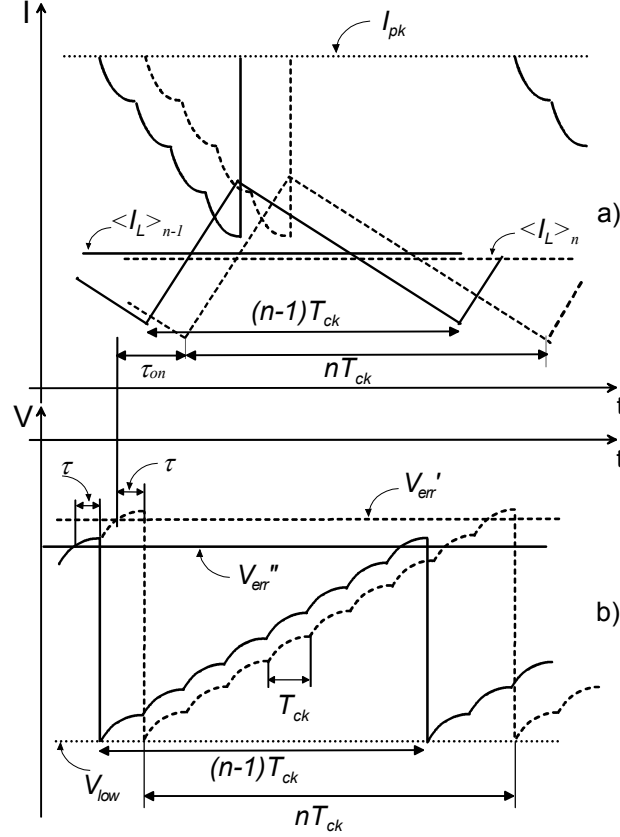


Fig.3 Current (a) and voltage (b) waveforms for two different switching periods separated by  $T_{ck}$ .

illustrated in Fig. 4, the converter can provide a continuous range of currents if there is an overlap among current intervals associated to adjacent current levels.

Overlap is ensured if:

$$\langle I_L \rangle_{n-1} - \langle I_L \rangle_n < LSB_{DACI} \quad (4)$$

that is, if:

$$LSB_{DACI} > \frac{V_{out}}{2L} T_{ck} \text{ , i.e., } SlopeI > \frac{V_{out}}{2L} \quad (5)$$

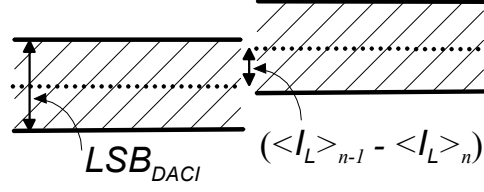


Fig.4 Overlap between current intervals associated to adjacent current levels.

In essence, if inequality 4 holds, the delay  $\tau$  and/or the switching period self adjust such that the average inductor current exactly matches the load current. The system has always a stable state thus preventing limit-cycle oscillations.

By means of this current self-regulation mechanism, the control system is able to react both to positive and negative load transients. The extent to which the average inductor current can be varied, however, depends on the allowed switching period interval,  $\Delta T_{sw}$ .

In practical systems, the switching period modulation must be limited to a small interval  $\Delta T_{sw} = \pm hT_{ck}$  centered around a nominal period  $T_{sw0}$ . If the allowed  $\Delta T_{sw}$  is not sufficient to guarantee the requested current variation, the peak current level  $I_{pk}$  generated by DACI must be correspondingly varied [7,8].

The digital controller updates the DACI output level by comparing the measured switching period  $T_{sw}$  with the nominal switching period  $T_{sw0}$ . In practice, the difference  $(T_{sw} - T_{sw0})$  is measured by counting the number of clock periods elapsed between the start and stop of the digitally generated voltage ramp. If  $(T_{sw} - T_{sw0})$  stays within the allowed  $\Delta T_{sw}$ , no action is taken. Otherwise, the DACI output is varied by a number of levels given by:

$$N_{update} = \frac{(T_{sw0} - T_{sw})}{T_{ck}} \quad (6)$$

As highlighted in ref. [8],  $(T_{sw} - T_{sw0})$  can be considered as the error signal of control system.

The control algorithm updates the peak current level proportionally to the switching period error, with a user-defined dead-zone  $\Delta T_{sw}$ . In essence, the digital control implements a proportional algorithm that acts to keep the switching period within the allowed range.

It is worth noting that the controller can be even operated at constant switching frequency, that is,  $\Delta T_{sw}=0$ . In this case, when the peak current level  $I_{pk}$  is kept fixed, the average inductor current  $\langle I_L \rangle$  can be continuously varied within an interval  $\Delta \langle I_L \rangle = SlopeI \cdot T_{ck}$ , by modulating the delay  $\tau$ . When  $I_{pk}$  is updated by one LSB at a constant  $\tau$ , the average inductor current is correspondingly increased/decreased by  $LSB_{DACI}$ . Overlap among current intervals associated to adjacent values of  $I_{pk}$ , i.e., current continuity, is ensured if:

$$\Delta \langle I_L \rangle = SlopeI \cdot T_{ck} > LSB_{DACI} \quad (7)$$

that is, if:

$$SlopeI > \frac{LSB_{DACI}}{T_{ck}} \quad (8)$$

Note that if  $SlopeI=LSB_{DACI}/T_{ck}$  there is contact, but no overlap, between two adjacent current intervals. The system works at the boundary between stable and unstable operation. In order to make the controller more robust,  $SlopeI$  must be at least doubled, i.e.,  $SlopeI=2 \cdot LSB_{DACI}/T_{ck}$ .

### C. Adaptive Voltage Positioning

Adaptive Voltage Positioning (AVP) [10], also known as “droop function”, can be easily included in our control system by forcing any variation of DACI to be tracked by a corresponding variation of DACV [7,8]. More precisely, if  $I_{pk}$  is increased by  $\Delta I_{pk}$ ,  $V_{low}$  should be correspondingly decreased by  $\Delta V_{low}$  and vice versa. In fact, a variation  $\Delta V_{low}$  of the voltage level  $V_{low}$  produces an identical variation  $\Delta V_{out}$  of the output voltage, since  $\Delta V_{out} = \Delta V_{err} = \Delta V_{low}$  (see equation 2).

In the present implementation, both DAC outputs are changed by the same number of levels, so that the droop resistance,  $R_{droop}$ , is given by [8]:

$$R_{droop} = \frac{\Delta V_{low}}{\Delta I_{pk}} = \frac{\Delta V_{out}}{\Delta I_{pk}} = \frac{LSB_{DACV}}{LSB_{DACI}} = \frac{SlopeV}{SlopeI} \quad (9)$$

Accordingly, the output voltage  $V_{out}$  is positioned at

$$V_{out} = V_{ref} - R_{droop} I_{out} \quad (10)$$

where the optimal value of  $R_{droop}$  is equal to the Equivalent Series Resistance (ESR) of the filter capacitor.

#### *D. Load regulation*

Load regulation analysis is similar to that given in ref. [8], with the only difference being the presence of the current ramp. Ideally, if the load current varies by  $\Delta I_{out}$ , the output voltage is expected to vary by:

$$\Delta V_{out} = -R_{droop} \Delta I_{out} \quad (11)$$

However, slight deviations from ideality are expected for small load variations, where DACV and DACI outputs are not changed and the output current is adjusted just by varying the switching period  $T_{sw}$ , and the delay  $\tau$ . In this condition, we obtain from equation 1:

$$\Delta \langle I_L \rangle = \Delta I_{out} = - \frac{V_{out}(1-D)}{2L} \Delta T_{sw} - SlopeI \cdot (D \cdot \Delta T_{sw} - \Delta \tau) \quad (12)$$

The small variations of  $V_{out}$  and  $D$  due to the AVP have been neglected, since they can be considered a second-order effect.

If ideal AVP were implemented, a variation of the switching period would cause a variation of the output voltage given by:

$$\Delta V_{out_{ideal}} = \Delta V_{err_{ideal}} = -R_{droop} \Delta I_{out} = \left( R_{droop} \frac{V_{out}(1-D)}{2L} + SlopeV \cdot D \right) \Delta T_{sw} - SlopeV \cdot \Delta \tau \quad (13)$$

In practice, a switching period variation,  $\Delta T_{sw}$ , produces an effective output voltage variation that can be easily calculated by differentiating equation 2:

$$\Delta V_{out_{effective}} = \Delta V_{err_{effective}} = SlopeV \cdot (\Delta T_{sw} - \Delta \tau) \quad (14)$$

The maximum error,  $\varepsilon$ , on the output voltage is therefore given by:

$$\varepsilon = (\Delta V_{out_{effective}} - \Delta V_{out_{ideal}}) = \Delta T_{sw} \cdot \left( SlopeV \cdot (1-D) - R_{droop} \frac{V_{out}(1-D)}{2L} \right) \quad (15)$$

A more detailed analysis shows that an additional contribution to the error arises from the non-linear shape of the current and voltage ramps. The magnitude of this contribution depends on the value of  $D$ ,  $\tau_{on}$ ,  $\tau_{off}$  and  $\tau$ , and it has a worst-case value of  $LSB_{DACV}$ . This is also true for the operation at fixed switching frequency ( $\Delta T_{sw}=0$ ).

### E. Controller design criteria

The most critical parameter to set is the clock period  $T_{ck}$ . It must be sufficiently high to allow the application of the control algorithm specified by equation 6. Since the switching period is discrete, the minimum width of the allowed switching period variation  $\Delta T_{sw}$  is given by  $2T_{ck}$ . Therefore:

$$\frac{\Delta T_{sw}}{T_{sw0}} \geq \frac{2T_{ck}}{T_{sw0}} \quad (16)$$

If we consider, for example,  $\Delta T_{sw}/T_{sw0} = \pm 5\%$  and  $T_{sw0}=2 \mu s$  ( $f_{sw0} = 500$  kHz), we obtain  $T_{ck} < 100$  ns ( $f_{ck} \geq 10$  MHz).

Once  $T_{ck}$  has been defined,  $LSB_{DACV}$  can be determined by setting a maximum limit to the voltage error  $\varepsilon$ . If, for instance,  $\varepsilon < 0.1\%$ ,  $R_{droop} = 5m\Omega$ ,  $V_{out} = 1.5$  V,  $D = 0.125$ ,  $L = 300$  nH,  $T_{ck}=30ns$  we obtain, from equation 15,  $LSB_{DACV} < 1.5$  mV. The size of  $LSB_{DACI}$  follows from equation 9. Once  $LSB_{DACI}$  is set, the inductance  $L$  must be suitably designed in order to satisfy inequality 5.

Details for proper design of  $V_{ref}$  and the zero-load value of  $V_{low}$  can be found in ref. [8]. Finally, the resolution in bits of DACI and DACV can be defined based on the output current dynamic of the converter and the value of the droop resistance.

### F. Extension to multiphase converters

A digitally controlled multiphase converter can be simply derived from the single-phase converter described above, by resorting to a master-slave architecture [8]. Each slave (phase) is a buck converter that receives two signals from the master controller: a reference current signal, generated by DACI and a turn-on signal. The slave is operated in peak-current mode: it turns off when the inductor current reaches the reference signal and it turns on when it receives the corresponding signal from the master controller. The master controller senses the output voltage level and activates one phase each time the error voltage  $V_{err}$  intercepts the DACV output voltage. Phases are activated cyclically. If there are  $N$  slaves, each slave works at a switching frequency of  $f_{sw}/N$ , where  $f_{sw}$  is the frequency of the voltage ramp produced by DACV. Due to this simple algorithm for phase activation, the switching period is an integer multiple of  $NT_{ck}$ . It follows that the separation between two adjacent average current levels (see equation 3) is given by:

$$\langle I_L \rangle_{k-1} - \langle I_L \rangle_k = \frac{V_{out}(1-D)}{2L} NT_{ck} + SlopeI \cdot (D \cdot N \cdot T_{ck}) \quad (17)$$

The converter can provide a continuous range of currents if inequality 4 is satisfied, that is, if:

$$SlopeI > \frac{N(1-D)V_{out}}{(1-N \cdot D)2L} \quad (18)$$

It is worth noting that inequality 18 cannot be satisfied for any value of  $SlopeI$  if  $ND > 1$ . However, in the most common applications  $D$  ranges from 10% to 20%, thus allowing for the control of multiphase converters with up to 5 phases. In order to avoid this limitation the controller may work at fixed frequency, hence the current can be continuously varied within an interval  $\Delta \langle I_L \rangle = SlopeI \cdot T_{ck}$  by modulating the delay  $\tau$ .

### III. EXPERIMENTAL RESULTS

The digital controller was tested on a prototype buck converter having the following parameters:  $C = 2\text{mF}$ ,  $ESR \sim 5\text{ m}\Omega$ ,  $L = 600\text{ nH}$ ,  $f_{swo} = 500\text{ kHz}$ ,  $V_{in} = 12\text{ V}$ ,  $V_{out} = 1.5\text{V}$ . AVP was programmed to obtain a droop resistance of about  $5\text{ m}\Omega$ . The control algorithm was developed in VHDL and then implemented into a FPGA device (Xilinx, Virtex XCV 50) operated at  $f_{ck} = 30\text{MHz}$ ; the whole digital circuit requires about 2000 equivalent gates. Two D/A converters (BurrBrown DAC2904) operating at 7 bits have been used for implementing DACI and DACV, with  $LSB_{DACI} = 170\text{mA}$  and  $LSB_{DACV} = 0.9\text{ mV}$ .

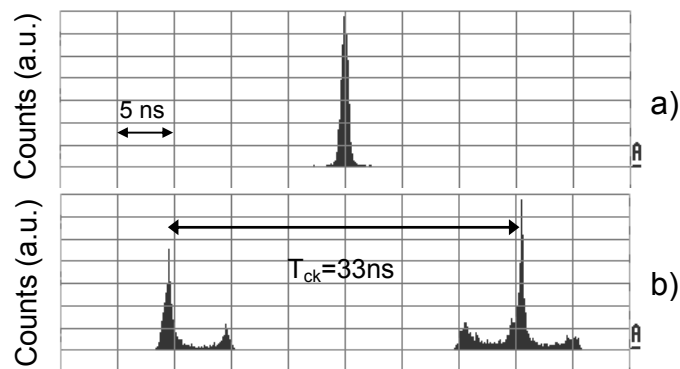


Fig.5 Time distribution of the switching period,  $T_{sw}$ : (a) current ramp enabled; (b) current ramp disabled.

We first performed steady-state measurements, in order to demonstrate the complete suppression of limit-cycles. Fig. 5a shows the histogram the switching period of the converter operating at a constant load current of  $5\text{ A}$ , with  $\Delta T_{sw} = \pm 3T_{ck}$ . The histogram collects about 20000 measurements. Note that the switching period is quite sharp: there is no evidence at all of the presence of limit-cycle effects. The same result has been obtained by varying the load current between  $0$  and  $15\text{ A}$  and by forcing different values of  $\Delta T_{sw}$ .

For comparison, we performed the same measurement by removing the current ramp. As shown in Fig. 5b, two peaks separated exactly by  $T_{ck}$  appear in the histogram. This is consistent with the conclusions drawn in ref. [8], where we showed that the converter is not

able to produce a continuous range of average inductor currents. When the load current does not match the discrete output current available from the converter, a limit cycle oscillation sets up. The switching period oscillates between  $mT_{ck}$  and  $(m+1)T_{ck}$  and the duty-cycle of the oscillation is such that the average inductor current balances the output current.

Fig. 6 shows the response of the converter to a slow load transient ( $3 \cdot 10^3$  A/s) of 10A. Measurements were performed by using an active load (Chroma mod.63102). Fig. 6a shows the current transient. Fig. 6b, c, d show, respectively, the output voltage transient with  $\Delta T_{sw} = 0$ ,  $\Delta T_{sw} = \pm T_{ck}$ ,  $\Delta T_{sw} = \pm 3T_{ck}$ .

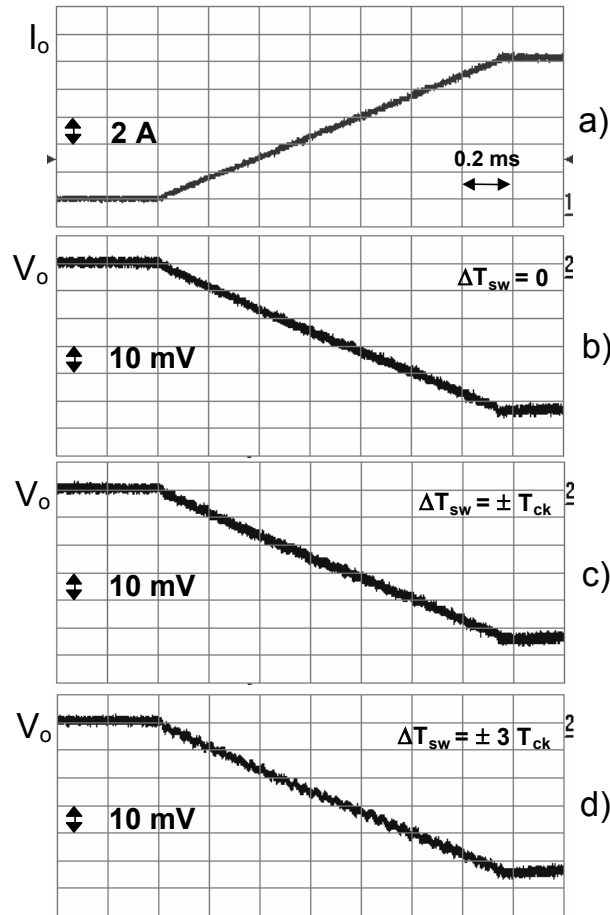
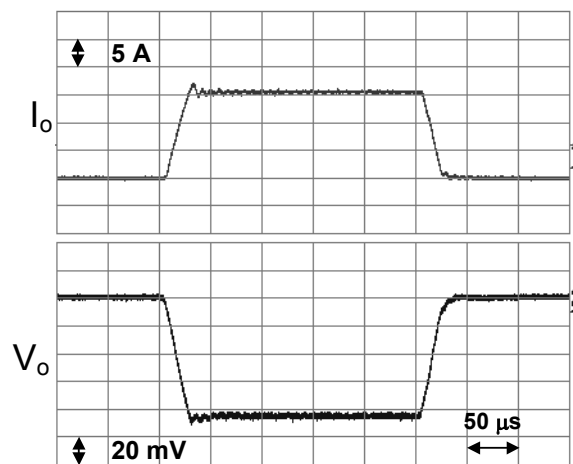


Fig.6 Response of the converter to a slow load transient of 10 A.

As expected, in all cases the average slope of the output voltage is consistent with the droop resistance. The response is almost ideal for the case  $\Delta T_{sw} = 0$ , while a small ripple (barely observable in Fig. 2c, more evident in Fig. 2d and 2e), is present when  $\Delta T_{sw} \neq 0$ . This ripple is

due to current regulation mechanism explained in Section II and its amplitude can be exactly predicted by using equation 15. It is worth noting that in all measurements the output voltage tolerance is well within  $\pm 0.5\%$  of the nominal value.

Fig. 7 shows the response of the converter to a fast load transient is from 0 A to 15 A. A nearly ideal voltage step of about 80 mV is generated in response to the transient. The limited current slew-rate and the small undershoot on the trailing edge of the output voltage waveform are due to the active load. It must be pointed out that, even with fast current transients, the output voltage tolerance stays within  $\pm 0.5\%$ .



*Fig. 7 Response of the converter to a fast load transient from 0A to 15 A.*

#### IV. INTEGRATION

Based on this new architecture, a VRM controller has been designed a monolithic by using the BCD VI (Bipolar, CMOS, DMOS) technology available from ST-Microelectronics. The controller is able to drive up to six phases and it is fully compliant with VRM10/11 Intel specifications. The block diagram of the controller is presented in Fig 8.

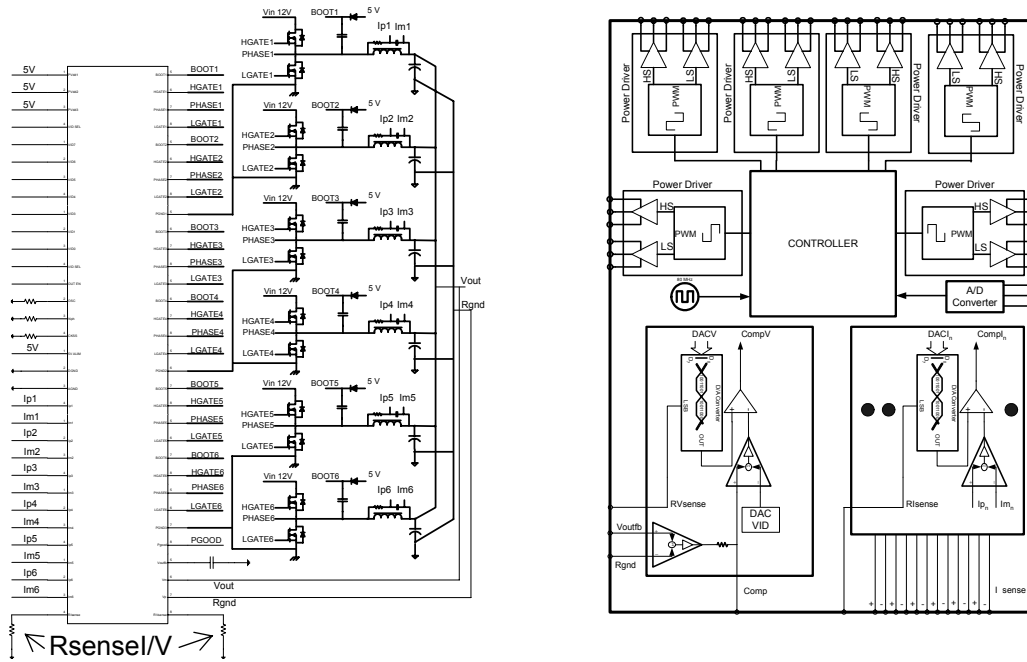


Fig.8 Application and block diagram of the controller

It has been used Seven D/A converters operating at 8 bits with adjustable LSB by choosing the two resistor  $R_{senseI/V}$ , indicated in Fig. 8, for implementing DACI (one for each phase) and DACV. In this way is possible to set up the maximum output current for each phase and the droop resistor of the VRM. Offsets of the analog front-end are compensated by an automatic test during the startup of the device. In this period the measure of offsets is obtained by measuring the zero-crossing of the comparators (COMPI, COMPV) while D/A converters are generating a ramp. To improve the accuracy performance the controller implements an A/D conversion of the distance from the peak current to the average current of each phase. The analog to digital conversion is implemented by the DACI during the  $T_{off}$  of the PWM wave.

The drivers for the power MOSFETs are included in the IC scheme, they work at 5V and use 37% of the total area of the controller. The others principal parts of the chip are: the analog part, which is large the 13.2% of the chip, and the digital part which is large the 13.1%, as described in Fig 9. The rest of the area is occupied by service blocks like the oscillator, VID

D/A converter, voltage and current references, PROM memory for precision trimming, pads and ESD protection.

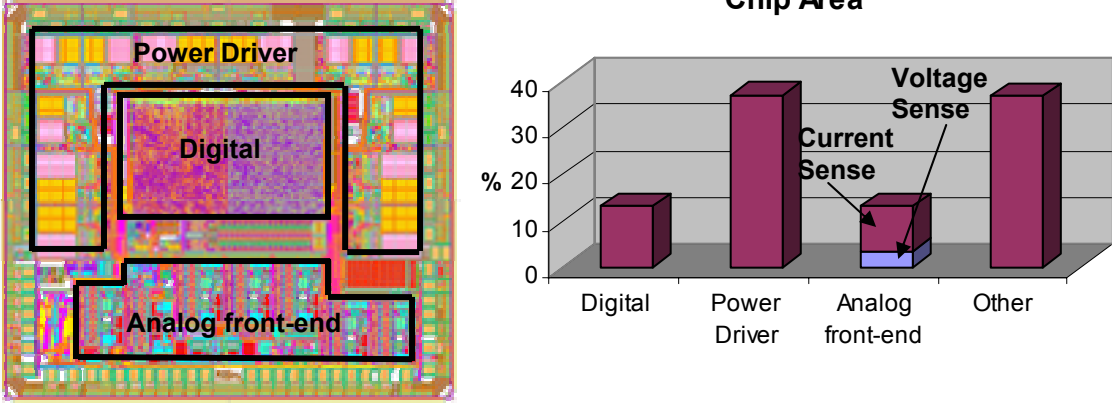


Fig.9 Floor plan and chip area consumption

### V. CONCLUSIONS

A mixed synchronous/asynchronous digital controller for DC-DC converters was proposed. The main features of the controller are: i) reduced complexity, thanks to the use of two low-resolution (7 bits) DACs; ii) control algorithm designed for suppressing quantization effects in spite of the low resolution; iii) fully reconfigurable digital architecture.

The control algorithm was developed in VHDL and synthesized to approximately 2000 equivalent gates into a small, commercially available FPGA. The main parameters of the controller (droop/no-droop, droop value, switching frequency, switching frequency tolerance) are fully programmable.

The digital controller was experimentally verified on a single-phase buck converter in order to validate the design approach and to demonstrate the key features. The suppression of limit-cycle oscillations, along with an output voltage tolerance within  $\pm 0.5\%$  and fast transient response was demonstrated.

The proposed digital control architecture can be easily extended to multiphase converters. The features and the performance of this architecture make it a valuable alternative for the control of DC/DC converters with tight voltage tolerance.

Finally an integrated realization in BCD 0.35 $\mu$ m technology of the controller has been illustrated.

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